snug world

SNUG World User Conference

AGENDA AT A GLANCE

TUESDAY | APRIL 20, 2021

	ARTIFICIAL INTELLIGENCE	AUTOMOTIVE	CLOUD	CUSTOM-AMS	DIGITAL DESIGN	EMULATION	FORMAL VERIFICATION	IP	LOWER POWER DESIGN	NEW VERIFICATION TECHNOLOGIES	PHYSICAL VERIFICATION	PROTOTYPING	SECURE, SAFE & RELIABLE	SIGNOFF I	SIGNOFF II	SILICON TEST & ANALYTICS	STATIC VERIFICATION	VCS/VERDI/VIP	VIRTUAL PROTOTYPING
7:00 - 7:25 AM		Building a Trustworthy Autonomous Vehicle (AV) Architecture																	
7:25 - 7:50 AM																			
10 MINUTE BREAK																			
8:00 - 8:25 AM		CNN Acceleration: A Short Road Trip																	
8:25 - 8:50 AM		Accelerate the Development of Dependable Automotive SoCs with Synopsys' Comprehensive Safety-Aware Solution																	
8:50 - 9:00 AM	CHAIR YOGA																		
9:00 - 9:50 AM	KEYNOTE: Welcome to a Bold New Era of Moore's Law																		
10 MINUTE BREAK																			
10:00 - 10:25 AM	Executive Panel: How Is AI Changing The Way We Approach Chip Design?	Influence of Dynamic Driving Model on SoC Development and IP Selection	Accelerating Semiconductor Design and Verification using Cloud Optimized EDA Solutions from Synopsys	Unleashing PrimeSim Continuum	Successful 2.5D and 3D Multi-die Silicon System Design using Synopsys' 3DIC Compiler and Ansys' Multiphysics Analysis	*Compile Time Improvements using Zebu zECO Flow for Debug Methodology			Energy Efficient Chip Design	Improving Verification Efficiency and Productivity with VC Portable Stimulus	Driving Physical Signoff Convergence at Advanced Technology Nodes		KEYNOTE: Zero Trust Microelectronics: A Model for Hardware Security Evolution	*Min-Max Contention Aware Clock Planning in Mega Hierarchical Designs	Cost-Effective Characterization on Arm based AWS Graviton2 Processors Using SiliconSmart®	TestMAX Manager for RTL-Based Test Flow	*Hierarchical CDC Verification on Billion Gates		
10:25 - 10:50 AM		Samsung Foundry's Automotive Reference Flow	Hybrid EDA Workloads in Public Cloud	Panel: The Future of Hardware for Circuit Simulation		*Emulation Model Optimizations: Improving Build, Runtime and Data Processing Performance for Benchmarking			Synopsys Low Power Solution, from Acritecture to Signoff		Shift-Left LVS Closure: IC Validator Explorer LVS			Small Range Hold Fixing with LoadCap Cell in PrimeTime	Hyper-scaled Library Characterization For Improved Turnaround Time	TestMAX Manager Flow for Scan Static Timing Analysis (STA) Optimization	*CDC Multi Mode Analysis		
10 MINUTE BREAK																			
11:00 - 11:25 AM	*Mozart – An HBM2-Based AI Accelerator	Replay: Building a Trustworthy Autonomous Vehicle (AV) Architecture	Optimizing EDA Workloads for SAFE-CDP A Novel Virtual Chip Design Environment on the Cloud	PrimeSim: Heterogeneous CPU and GPU Technology Delivers Order-of-Magnitude Performance Breakthrough	Getting the Most out of Fusion Compiler with RM 2.0	*Achieving 2-3X Execution Throughput Improvement using Zebu Latest Features and Design Optimization Techniques			Billion Gates Power Analysis Using Emulations	Euclide: Finds Bugs Early to Accelerate Design and Verification Productivity	IC Validator Based Physical Verification Methodology for High Full Flow Productivity		Challenges and Approaches to Secure Hardware Design	*50% Reduction in TAT Using Signoff-driven ECO Closure	Unified Library Characterization and Validation Solution Targeting Advanced Nodes	*A Hybrid ATPG and Logic BIST Architecture for Extreme Compression	*Efficiently Solving the Challenges of Clock and Reset Domain Crossing Verification for Large SoCs	Delta Glitch - Chasing and Resolving	
11:25 - 11:50 AM	*AI Based Design: Challenges and Methodology for Best PPAv		*Migrating VLSI Infrastructure to AWS – Challenge Accepted	Game Changer- GPU Simulator for AMS Design	*The Next Level of Fusion: Fusion Technology™ + EMLL + Design Services	Fast Forward Your Software Development with Advanced Hybrid Technologies			SAM Based Full Chip Multi-Voltage Verification in VC LP	AI-powered Efficient Debug with Verdi	*Full Chip Antenna DRC Runtime Challenges and Solutions		Keeping Old Tech Alive - A Robust Flow for Recreating Obsolete Components Using FPGAs	*Next Big Break Through in Optimization Arena		*Migrating to Fusion Compiler™ from Design Compiler, Design-for-Test & IC Compiler II Has Never Been so Easy!	*Metastability Bugs Prevention via CDC and RDC Verification: Learnings from SoC Design	*UVM DUT Harness Verification Technique. .Minus the Harness!	
10 MINUTE BREAK																			
12:00 - 12:25 PM	*Edge AI Inference SoC Physical Design Challenges & Methodology to Achieve Best PPA	Replay: CNN Acceleration: A Short Road Trip	Scaling DSO.ai on Microsoft Azure	Flexible and Feature Rich Simulation Cockpit for Netlist	Achieving the Best PPA on Advanced Arm® Cores with Synopsys' Fusion Design Platform™	*Optimizing Firmware Performance of an NVMe-based SSD on Zebu Hardware Emulation Platform			The New AI Frontier – Breaking Down Power Barriers	Driving Efficiency & Productivity in SoC Verification Sign-off with Unified Verification Management Automation	*Secure Lynx-Based Cloud Design Environment Enabling Accurate and Efficient Physical Verification and Fabrication Sign-Off		A Framework for Assessing the Vulnerability of ICs Against Fault Injection Attacks	Estimating DVD-Induced Timing Impact Using PrimeTime® and RedHawk-SC		New Pattern Conversion Technology using EDA Solution	*Scalable RDC Signoff Methodology for Large SoCs	Catching Bugs Early with Dynamic Simulation	
12:25 - 12:50 PM	Case Study for AI SoC IP: Emerging Neural Network's Drive Innovation	Replay: Accelerate the Development of Dependable Automotive SoCs with Synopsys' Comprehensive Safety-Aware Solution		Design migration and Simulation Challenges Getting Resolved in Enabling Custom Compiler for 7nm Platform					*Pre-Silicon Functional and Power Validation Using Gate-Level Emulation		High Performance Layout Analysis with IC Validator Workbench		DoD State-of-the-Art Enterprise Hardware Emulation	PrimeTime® Technologies for Designers' Productivity		Fusion of Next-Generation RTL-to-GDSII Solution and Advanced DFT Technology	*The Latest Advancements in Preventing Reset Domain Crossings Bugsy	Powerful Debug of Complex Constraints During VCS Simulation	
10 MINUTE BREAK																			
1:00 - 1:25 PM				Ensuring Functional Safety of Memory IP using PrimeSim CustomFault									Secure Semiconductor Development - Design Challenges and Reasonable Practices						
1:25 - 1:50 PM				Using PrimeSim HSPICE StatEye with IBIS-AMI Models for DDR5 and LPDDR5 SI Analysis															
10 MINUTE BREAK																			
2:00 - 2:50 PM	ENTERTAINMENT - Virtual Deceptions with Magician Dennis Kyriakos																		

WEDNESDAY | APRIL 21, 2021

	ARTIFICIAL INTELLIGENCE	AUTOMOTIVE	CLOUD	CUSTOM-AMS	DIGITAL DESIGN	EMULATION	FORMAL VERIFICATION	IP	LOWER POWER DESIGN	NEW VERIFICATION TECHNOLOGIES	PHYSICAL VERIFICATION	PROTOTYPING	SECURE, SAFE & RELIABLE	SIGNOFF I	SIGNOFF II	SILICON TEST & ANALYTICS	STATIC VERIFICATION	VCS/VERDI/VIP	VIRTUAL PROTOTYPING
7:00 - 7:25 AM		Facilitating Distributed Development of Safety Critical Automotive IP and SoC																	
7:25 - 7:50 AM																			
10 MINUTE BREAK																			
8:00 - 8:25 AM		Replay: Ensuring Functional Safety of Memory IP using PrimeSim CustomFault																	
8:25 - 8:50 AM		Analog Fault Simulation for ISO 26262 using PrimeSim CustomFault																	
8:50 - 9:00 AM	GUIDED MEDITATION																		
9:10 - 9:50 AM	KEYNOTE: Architecting the Next 100B Intelligent Devices																		
10 MINUTE BREAK																			
10:00 - 10:25 AM	Replay: Executive Panel: How is AI Changing the Way We Approach Chip Design?	Safety Critical Lint Methodology or Automotive Customer	VC Formal Seamless Scaling on AWS SOCA: A Winning Formula to Shift-Left Verification	Simulation Environment Update	Simply Better RTL: Enabling Shift Left Strategy with RTL-Architect	*Enabling External Customer to use NXP's In-House Zebu Emulation Setup to meet Pre-Silicon Verification Milestones		Die-to-Die Connectivity - Trends, Use Cases, Requirements	Panel: End to End Low Power Solution Panel		Free PDK3: A Novel PDK for Physical Verification at the 3nm Nodes			*Using PrimeShield Variation Analysis to Create a More Robust Core, at Fraction of the Cost of Flat Margins	Efficient Post-Layout Simulation and EMIR Validation with StarRC™ GPD Flow	TestMAX Advisor – Boost Coverage and Reduce Pattern Count Today!	*Noise Reduction using Static and Formal Aware Linting in a Single Phase	Increase Coverage, Reduce TAT with VCS Intelligent Coverage Optimization – Driving Verification Efficiency with AI/ML Innovation	*Virtualized CPU Usage in SoC Verification
10:25 - 10:50 AM		Methodological Approach to Fault Injection Campaign Measurements	Containerization for EDA Workloads	Faster Analog Design Closure with Early Parasitic Analysis Flow in Synopsys Custom Design Platform		*Network Switch Pre-Silicon Debug using ZeBu Record and Replay		A Seamless Transition to PCIe 6.0 Designs with Optimized IPs			Enabling your Designers with IC Validator Launch			*Design Variation Analysis and Variation Robustness Using STA based Monte Carlo	*QuickCap Parasitic Extraction for Arm Physical Design	*RTL Design Validation Using Static Connectivity Checks	*Link Abstract Flow – A Hierarchical Approach to Enhance RTL-checking Quality with Faster Turn-around	*Refine the Tests Portfolio using VCS Coverage and Test Grading	*System-Level Power Modelling for Processor Cores in Virtualizer
10 MINUTE BREAK																			
11:00 - 11:25 AM	Getting Started with DSO.ai™: A Tutorial	Replay: Facilitating Distributed Development of Safety Critical Automotive IP and SoC	Design Processing and Verification Using Kubernetes Based Hybrid Cloud Infrastructure	Improved QoR and Productivity for Analog Layout with Custom Compiler's Visually-Assisted Layout Automation	*Fast RTL Prototyping and PPA Exploration Using RTL Architect	Leading 800G Ethernet SoC Validation		Deciphering the MIPI Standards for Camera and Display	*Enable Level Shifter Insertion with Multiple Power and Bias Domains		Accelerating Physical Signoff Convergence for 5nm and 7nm Designs			*Parametric Timing Success-Rate Improvement using PrimeShield	Buried Signal Line Exploration for sub-5nm SRAM Design	RTL Based DFT Partition Scan Architecture	Noise Reduction in VC Spyglass Platform with Machine Learning and Formal Technology	*Automatic Functional Coverage Generation	Hybrid Emulation – Accelerate Software Enablement for Automotive SoC
11:25 - 11:50 AM	Towards Auto-Convergence in Digital Design: Using DSO.ai™ to Maximize PPA Benefits		Google Hardware Team's Cloud Journey	Template Based Analog Layout Flow at SK Hynix	Achieving Best Quality RTL for Faster Design Closure with Features-Added Physical Aware Synthesis (FPAS)	Staying Ahead in 5G System Verification		An Insight into the Evolution of HBM3	*How to Achieve the Best PPA on an Ultra-Low Power STM32 Microcontroller, SAIF Driven Synthesis Flow		Advanced Reliability Checking with IC Validator PERC			PrimeShield Design Robustness Analysis and ECO	Extraction Innovations for Advanced Node Digital Design	Demonstration of TestMAX SMS Memory Test & Repair Flow!	A Comprehensive UPF Coverage Methodology to Avoid Late SI Issues	*Optimizing Test Execution Time for Coverage!	Early Software Development on a First Generation AI Chip with Virtualizer
10 MINUTE BREAK																			
12:00 - 12:25 PM	AI-Driven Design Space Optimization Case Study	Replay: Ensuring Functional Safety of Memory IP using PrimeSim CustomFault	Synopsys Testcase Packager: Seamless Migration and Execution for EDA Workloads on Cloud	Standard Cell Design Productivity Improvement with with Layout Editor Assisted Layout Automation	Case Study: Optimize and Configure Synopsys DesignWare IP with RTL Architect	*Low Power Emulation of Automotive SoC		Key Applications for In-Chip Sensing & PVT Monitoring	*Innovative Solutions for Complex Hierarchical UPF Design Implementations		*Synopsys ICV Live Enablement in IBM Advanced Node Processor Design Environment					Utilizing TestMAX SMS Algorithm Programmability to Reduce Unnecessary Timing Signoff Effort on Dual Port Memories		*Optimizing PCIe System-Level Performance in a Pre-Silicon Environment	Virtual Prototyping for Continuous Integration Testing of Embedded SW stacks
12:25 - 12:50 PM	*Machine Learning Based Root Cause and Power Aware Analysis in Asynchronous Design	Replay: Analog Fault Simulation for ISO 26262 using PrimeSim CustomFault		Accelerate Chip Integration While Improving SPEF Quality for Timing Closure with the Custom Compiler Solution	Formality ECO: Automated Functional ECOs with Hand-Crafted Quality and Minimal Effort			*PCIe RAS DES Framework for SoCs			*Tower Support for Synopsys' Analog / RF / Photonics Design Flows					Innovative Design-for-Test (DFT) Methodology for AI & Automotive SoCsy		Automation Accelerates Verification Closure upto 10X for next-gen SoCs- Simple, Scalable, & Efficient	
10 MINUTE BREAK																			
1:00 - 1:25 PM	*Unsupervised Machine Learning Based Root Cause Analysis of Front-End and Back-End Low Power Issues			Samsung AMS Design Reference Flow for Advanced Node												Memory Test and Repair and Hierarchical DFX Management of IP in Automotive and AI SoCsy			
1:25 - 1:50 PM				Replay: Tower Support for Synopsys' Analog / RF / Photonics Design Flows															
10 MINUTE BREAK																			
2:00 - 2:30 PM	ENTERTAINMENT - Dueling Piano Performance by Shellshocked																		

THURSDAY | APRIL 22, 2021

	ARTIFICIAL INTELLIGENCE	AUTOMOTIVE	CLOUD	CUSTOM-AMS	DIGITAL DESIGN	EMULATION	FORMAL VERIFICATION	IP	LOWER POWER DESIGN	NEW VERIFICATION TECHNOLOGIES	PHYSICAL VERIFICATION	PROTOTYPING	SECURE, SAFE & RELIABLE	SIGNOFF I	SIGNOFF II	SILICON TEST & ANALYTICS	STATIC VERIFICATION	VCS/VERDI/VIP	VIRTUAL PROTOTYPING
7:00 - 7:25 AM		GLOBALFOUNDRIES® 22FDX® Automotive Digital Design Flow Designing Functional Safety Features																	
7:25 - 7:50 AM																			
10 MINUTE BREAK																			
8:00 - 8:25 AM		*Mitigating Soft Errors Impact on System Reliability																	
8:25 - 8:50 AM		Replay: Innovative Design-for-Test (DFT) Methodology for AI & Automotive SoCs																	
8:50 - 9:00 AM	BREATH WORK																		
9:05 - 9:50 AM	KEYNOTE: Developing Next Generation Automotive Computing Platforms Based on a New Value Chain																		
10 MINUTE BREAK																			
10:00 - 10:25 AM		Safe, Secure, Everywhere: ISO 26262 Compliance for Modern Automotive Software		STMicroelectronics Memory Verification Flow Optimization Using Synopsys AMS Solutions	Automating Complex, High-Speed, Interconnect Planning for Next Generation Designs		*Instruction Set Verification using Automation and Formal Data Path		Fusion Based Methodology to Target Peak IR-Drop Reduction Throughout the Implementation Cycle		Physical Verification Strategies to Scale New-Age Complex Processes and Designs Challenges	*PCIe Gen5 at Speed End-to-End FPGA Prototyping with PHY Daughter Card		*Tweak-Your-ECOs "Efficient Way to Generate ECOs"	*Functional Equivalence Check of Industry's first eMRAM using Synopsys' ESP	*Using Synopsys Functional High-Speed Interfaces for SCAN Test		Replay: What's New in VCS co-simulation with AMS	
10:25 - 10:50 AM		The Future of Automotive Linux: Standardization and Safety		Performing MOS Reliability Analysis with Variability Using Advanced Monte Carlo Solutions	Replay: Getting the Most out of Fusion Compiler with RM 2.0		Out-of-the-box Performance Impact on Formal Verification Adoption Journey		Fixing IR Violations Using RedHawk Analysis Fusion with Fusion Compiler™		*Development of Superconductor Advanced Integrated Circuit Design Flow using Synopsys Tools	PCIe Gen5 Validation: The Real World		*Decrypting Paradox of Timing Issues with Tweaker	*A Novel Verification Methodology for Ring Oscillators using ESP	Automated Inking with Silicon Dash in Marvell		Replay: *A Framework for Assessing the Vulnerability of ICs Against Fault-Injection Attacks	
10 MINUTE BREAK																			
11:00 - 11:25 AM		Replay: GLOBALFOUNDRIES® 22FDX® Automotive Digital Design Flow Designing Functional Safety Features		*Cosim Using VCS PrimeSim AMS in FLASH Memory Drive	*RFSoC Block I/O Optimization		Unique and Advanced Formal Datapath Validation		Power Integrity and Timing Closure Shift Left with Joint Ansys/Synopsys Customer Solutions		*Using ICV 3D-IC Verification to Flag Incorrect Die Orientation and Bump Alignment in a Multi-Die Design	Getting the Most from your Prototyping Farm		*Bringing Full Chip Leakage Reduction into Reality	*Formal Verification for Mixed Signal IPs Using ESP: IO Perspective	Wafer Sort Parameters Post Processing for Assembly Inkless Map Generation		Testbench Debug Made Easier with Verdi	
11:25 - 11:50 AM				Improving Productivity and Ease-of-use of COSIM Setup for Analog-centric Users	*Frequency vs Time Done Right – Designing a High-Performance ARM POP IP Solution with Minimal Turn-around Time Using Synopsys Fusion Compiler™		Is Formal Signoff a Reality?		*Leakage Recovery Runtime Reduction		Replay: Design Processing and Verification Using Kubernetes Based Hybrid Cloud Infrastructure	Replay: *Keeping Old Tech Alive - A Robust Flow for Recreating Obsolete Components using FPGAs		*Timing Convergence with Velocity, Quality and Predictability	Validating Memory Design Scan Chains from Behavioral to Transistor Level	SiliconDash - The Next Generation High-Volume Semiconductor Big Data Analytics Solution		*Known Issues And Solutions (KIAS): A Way to Capture Solutions of Already Debugged Issues and Present as Information to Users Whenever Error is Logged Again	
10 MINUTE BREAK																			
12:00 - 12:25 PM		*Replay: Mitigating Soft Errors Impact on System Reliability		Advanced Custom Design & 3DIC Capabilities for Extraction	*Convergence Methodology & Optimization Techniques for Complex SoC Channel				Chip Level Standard Cell EM Signoff on SoC in PrimePower					Tweaker ECO Technology Innovations for Fastest Path to PPA Closure		Implementation and Use of PVT Monitors in Large Die Applications		*Fast Coverage Prototyping/Debug Using Waveform Data and Jupyter Notebooks	
12:25 - 12:50 PM		Replay: Innovative Design-for-Test (DFT) Methodology for AI & Automotive SoCs		Radically Improving Layout Efficiency Through the Use of User Defined Devices (UDD)	Replay: *The Next Level of Fusion: Fusion Technology™ + EMLL + Design Services				RTL Power Estimation Accuracy - Correlation Study						NanoTime Signal Integrity for Advanced Process Nodes	Introduction to Embedded In-Chip Sensing & PVT Monitoring		Beyond RAL - Improved Solutions for Advanced Registers Structures	
10 MINUTE BREAK																			
1:00 - 1:25 PM					Replay: *Migrating to Fusion Compiler™ from Design Compiler, Design-for-Test & IC Compiler II Has Never Been so Easy!				RTL Power Exploration with PrimePower RTL							The Lastest Techoloy Updates for Failure Analysis Solution of Samsung Foundry Silicon			
1:25 - 1:50 PM																Yield Explorer Introduction: Logic and Memory Volume Diagnostics			

ENTERTAINMENT ON-DEMAND: Technically Funny Comedy Break & Music Break with DJ Gatsby 6