2021 IEEE Radio Frequency Integrated Circuits Symposium

20–25 June 2021 ▪ Virtual

PROGRAM

Sponsored by

IEEE Microwave Theory and Techniques Society
IEEE Electron Devices Society
and
IEEE Solid-State Circuits Society

RFIC Virtual Event

20–25 June 2021

Sunday 20 June 2021, 10:00–12:00 EDT: RFIC Symposium Showcase

Sunday 20 June 2021, 12:00–15:00 EDT: Three Minute Thesis (3MT)

Monday 21 June 2021, 10:00–12:00 EDT: The RFIC/IMS Joint Plenary Session includes an overview of the conference and then talks by two outstanding speakers: Prof. Bram Nauta (Distinguished Professor at University of Twente) and Asha Keddy (Corporate Vice President and General Manager at Intel). Prior to the plenary, we will announce the RFIC awards.

Two more plenary talks will be available as pre-recorded videos by Dr. Ahmad Bahai (Chief Technology Officer and Senior Vice President at Texas Instruments) and Suresh Venkatarayalu (Chief Technology Officer at Honeywell).

Monday 21 June 2021, 12:30–14:00 EDT: Technical Lecture

Tuesday 22 – Thursday 24 June 2021, 10:00–11:40 EDT: RFIC Technical Sessions

Tuesday 22 – Thursday 24 June 2021, 11:40–12:30 EDT: Author Lounge Sessions

Tuesday 22 – Thursday 24 June 2021, 12:00–13:30 EDT: Technical Lectures

Tuesday 22 – Wednesday 23 June 2021, 13:00–14:30 EDT: Panel Sessions

Wednesday 23 June 2021, 09:00–16:30 EDT: Connected Future Summit

Thursday 24 June 2021, 12:30–14:00 EDT: RFIC Systems and Application Forum

Friday 25 June 2021, 10:00–16:00 EDT: RFIC Workshops

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RFIC Virtual Event Schedule (20–25 June 2021)

Event	Sun 20 June	Mon 21 June	Tue 22 June	Wed 23 June	Thu 24 June	Fri 25 June
RFIC Symposium Showcase	10:00–12:00					
Three Minute Thesis	12:00–15:00					
Plenary Session		10:00–12:00				
Connected Future Summit				09:00–16:30		
RFIC Technical Sessions			10:00–11:40			
Author Lounge Sessions			11:40–12:30			
Technical Lectures		12:30–14:00	12:00–13:30			
Panel Sessions			13:00–14:30			
RFIC Systems & Application Forum					12:30–14:00	
RFIC Workshops						10:00–16:00

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Welcome Message from Chairs

We invite you to join us for the *2021 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*. The RFIC Symposium is the premier IC conference focused exclusively on the latest advances in RF, millimeter-wave, and high-frequency IC technologies and designs. The Symposium, combined with the International Microwave Symposium (IMS), ARFTG, and the Industry Exhibition, forms "Microwave Week", the largest RF and microwave technical meeting of the year. This year, to maximize our community's ability to participate, we are organizing the Symposium as a first-ever hybrid event with both in-person and virtual symposiums. Our goal for both events is to ensure safe, informative, interactive, and effective events for all participants.

This book presents our virtual symposium technical program; however, we first summarize the in-person plans. The in-person RFIC Symposium has been merged with the in-person IMS, taking place in Atlanta, GA at the Georgia World Congress Center on Monday through Wednesday, 7–9 June 2021. The event starts with a complimentary lecture program on Monday. On Monday night, there will be a plenary session followed by a welcome reception. Two outstanding industry leaders will give the plenary talks — Dr. Ahmad Bahai, the chief technology officer from Texas Instruments and Mr. Suresh Venkatarayalu, the chief technology officer from Honeywell. RFIC and IMS technical sessions will be held on Tuesday and Wednesday in parallel tracks featuring authors who elect to attend in person. Finally, the IMS technical exhibition will be held on Tuesday and Wednesday.

The virtual RFIC Symposium will start two weeks after the in-person event, running from Sunday, 20 June 2021 through Friday, 25 June 2021. Attendees will use an on-line platform, vFairs.com, to access content and interact with others. Note that all attendees of our in-person symposium will receive complimentary access to the virtual symposium. For the virtual program, all presentations, workshops, lectures, and panels will be *live-streamed* by presenters and then available on demand for one month. Most sessions are scheduled to begin at 10:00 EDT to maximize the ability for attendee participation from around the world.

On Monday, 21 June 2021, a live-streamed joint RFIC/IMS Plenary Session will be held, featuring prominent speakers from the RF and microwave fields. Dr. Bram Nauta, Distinguished Professor at the University of Twente, The Netherlands, will present a forward-looking talk on his "*Transceiver Roadmap for 2035 and Beyond*", where we will learn from him what the RF transceiver may look like fifteen years from now and the research needed to get us there. Additionally, videos captured from our in-person plenary talks will be presented, including the talk from Dr. Ahmad Bahai, Chief Technology Officer and Senior Vice President at Texas Instruments. His talk on "*New Horizons for Millimeter-Wave Sensing*" will provide an overview of the rapidly evolving mmWave sensor market, including radar, imagers, and spectroscopy, and the research and development opportunities at device, packaging, system, and algorithm levels.

Fourteen RFIC technical sessions will be held on Tuesday, Wednesday, and Thursday, in parallel tracks, and will feature live-streamed talks from all RFIC authors. Each session will include time devoted to questions and answers in an "author lounge". Our sessions will include topics spanning from highly-integrated wireless systems-on-chip and low-power radios to new phased arrays, power amplifiers, voltage-controlled oscillators, and front-end circuitry. Continuing in 2021, the RFIC Symposium has an expanded scope that includes RF Systems and Applications related to novel applications of RFICs at the systems level. This is reflecting the fact that more research challenges are being addressed at higher levels through new architectures, new usage models, new calibration techniques, and new integration approaches. Additionally, in 2021 we continue with an expanded scope that includes emerging technologies in RF, such as quantum computing, optoelectronics, MEMs, hardware security, and machine learning.

The virtual 2021 RFIC Symposium will feature a rich and diverse educational program, including four technical lectures, accessible to all RFIC attendees at no additional charge, and 12 workshops. Technical lectures are intended for newcomers and practicing designers alike. They include lectures on power amplifiers by Dr. Peter Asbeck, sensing radars by Prof. Jenshan Lin, terahertz imaging and spectroscopy by Prof. Ehsan Afshari, and mm-wave wireless fiber by Prof. Amin Arbabian. The lectures will be live-streamed on Monday through Thursday afternoons. Additionally, RFIC workshops will be live-streamed on Friday, 25 June 2021, including both half-day and full-day options. They cover a comprehensive range of advanced topics in RF technology and design, including power amplifiers, 5G systems, coherent optical links, terabit/s networks, quantum computing, imaging radars, and much more.

Two live-streamed panels are scheduled for Tuesday and Wednesday, 22–23 June 2021. In the first, panelists will debate the topic "*RFIC Startups: A Dead Horse in the Era of Software Unicorns and Pandemics?*" to help both students and aspiring entrepreneurs understand the evolving RF start-up landscape in today's economy. In the second, panelists will discuss the topic of "*Automotive Radars and AI: Is My Car Really Safe?*" debating the roles of RF circuits and AI in enabling autonomous driving. Additionally, on Thursday, 24 June 2021, we will feature a new systems and application forum at the virtual event to highlight short videos of RFIC authors' circuit and system demonstrations.

RFIC 2021 and Microwave Week have many opportunities for students. Students can register for the symposium and workshops at greatly discounted rates. Second, RFIC will offer NSF-sponsored registration/travel awards to select students from US-based universities, covering all conference costs. Third, RFIC will conduct a contest to select the top student papers from the symposium. Fourth, students and professionals have the opportunity to apply for and participate in the Three-Minute Thesis (3MT®) program, held virtually this year.

On behalf of the RFIC Steering, Executive and Technical Program Committees, we welcome you to join us at the 2021 RFIC Symposium! Please visit the RFIC 2021 website (https://rfic-ieee.org/) for more details and updates.

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General Chair
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Osama Shana'a
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RFIC Virtual Event (20–25 June 2021)
Session List

Sunday, 20 June 2021

10:00–12:00 RFIC Symposium Showcase
12:00–15:00 Three Minute Thesis (3MT)

Monday, 21 June 2021

10:00–12:00 RFIC/IMS Joint Plenary Session
12:30–14:00 Technical Lecture by Peter Asbeck — *A Tour Through the World of Si IC Power Amplifiers*

Tuesday, 22 June 2021

10:00–11:40 RTu1E — *Circuits and Systems for Microwave and mm-Wave Sensing, Radar and Communications*
RTu1F — *High Performance mm-Wave Front-End Circuits*
RTu1G — *Advanced Techniques for Power Amplifier Modules, Sub-THz and BIST*
10:00–11:20 RTu4F — *High-Performance Fractional-N PLLs and Building Blocks*
12:00–13:30 Technical Lecture by Jenshan Lin — *Micro-Motion Sensing Radar: Theory, System Architectures, and Circuit Implementations*
13:00–14:30 RFIC/IMS Joint Panel Session — *RFIC Startups: A Dead Horse in the Era of Software Unicorns and Pandemics?*

Wednesday, 23 June 2021

10:00–11:40 RTu1H — *Advanced N-Path Techniques and Associated Interference Mitigation*
RTu2E — *mm-Wave Circuits for 5G Systems*
10:00–11:20 RTu2F — *mm-Wave and Sub-THz Power Amplifiers*
10:00–11:40 RTu2G — *Circuit Techniques for High-Speed Transceiver Front-Ends*
RTu2H — *New Design Techniques for Frequency Generation*
12:00–13:30 Technical Lecture by Ehsan Afshari — *Fully Integrated Terahertz Imaging and Spectroscopy: From Device to System*
13:00–14:30 RFIC Panel Session — *Automotive Radars and AI: Is My Car Really Safe?*

Thursday, 24 June 2021

10:00–11:20 RTu3E — *CMOS Transmitters and Amplifiers from RF to mm-Wave*
RTu3F — *RF and mm-Wave VCOs*
RTu3G — *RF Systems for Emerging Wireless Applications*
RTu4E — *mm-Wave Circuits for Emerging Applications*
10:00–11:40 RTu4G — *Efficient Radios for IoT, GPS, WiFi, and Cellular*
12:00–13:30 Technical Lecture by Amin Arbabian — *mm-Wave "Wireless Fiber" to Meet the Capacity Demands of Future Networks*
12:30–14:00 RFIC Systems and Application Forum

Friday, 25 June 2021

10:00–14:00 RFIC Half-Day Workshops
10:00–16:00 RFIC Full-Day Workshops

RFIC/IMS Joint Plenary Session

Monday, 21 June 2021
10:00–12:00

General Chairs
RFIC: Brian Floyd, North Carolina State University
IMS: James Stevenson Kenney, Georgia Tech
John Papapolymerou, Michigan State University

TPC Chairs
RFIC: Osama Shana'a, MediaTek
Donald Y.C. Lie, Texas Tech University
IMS: Hua Wang, Georgia Tech
Debabani Choudhury, Intel

10:00 Welcome Message from General Chairs and TPC Chairs

10:30 *Transceiver Roadmap for 2035 and Beyond*
Prof. Bram Nauta
Distinguished Professor at University of Twente

11:00 *5G and Beyond: Enabling a Fully Connected, Mobile, and Intelligent Society over the Next Decade*
Asha Keddy, Corporate Vice President and General Manager at Intel

Additional plenary talks from the in-person event available as video-on-demand:

11:30 *New Horizons for Millimeter-Wave Sensing*
Dr. Ahmad Bahai
Chief Technology Officer and Senior Vice President at Texas Instruments

11:30 *Reimagine the Future — Smart & Connected Solutions*
Suresh Venkatarayalu
Chief Technology Officer at Honeywell

RFIC Plenary Speaker 1

Prof. Bram Nauta
Distinguished Professor
University of Twente

Transceiver Roadmap for 2035 and Beyond

Abstract: During the past decades wireless communication has made an enormous growth. Triggered by a large R&D effort, the integration of transceivers in CMOS technology has made low-cost mass production possible. For many applications like Bluetooth, a single-chip CMOS transceiver can now do the job. On the other hand, for complex transceivers like in modern smartphones, still more discrete RF components such as filters, switches and diplexers are being added to protect the transceiver from strong interferers which are often produced by the device itself. To satisfy the future bandwidth hunger, the number of frequency bands will further increase, modulation schemes will become more complex, more antennas will be used and carrier aggregation will be the norm. To limit the number of discrete RF components, linearity of the transceivers is key. Since more computing power will be needed in future transceivers as well, newer CMOS technologies are also wanted. CMOS technology will scale in favor of fast-switching digital circuits, but not for classical analog functions, like amplifiers. For the next fifteen years re-thinking of basic circuits and systems will be needed to make highly integrated linear transceivers, in a technology that is designed for digital circuits.

About Prof. Bram Nauta

Prof. Bram Nauta received the M.S. and Ph.D. degrees in electrical engineering from the University of Twente, Enschede, The Netherlands in 1987 and 1991, respectively. From 1991 to 1998 he worked at the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven, The Netherlands. In 1998 he returned to the University of Twente, where he is currently a distinguished professor and head of the IC Design group. His current research interest is high-speed analog CMOS circuits, software defined radio, cognitive radio, and beamforming. He has served as the editor-in-chief of the IEEE Journal of Solid-State Circuits, the president of the IEEE Solid-State Circuits Society, and on the technical program committees for many conferences. He is fellow of the IEEE and member of the Royal Netherlands Academy of Arts and Sciences (KNAW).

RFIC Plenary Speaker 2

Dr. Ahmad Bahai
Chief Technology Officer and Senior VP
Texas Instruments

New Horizons for Millimeter-Wave Sensing

Abstract: This talk will provide an overview of the rapidly evolving millimeter-wave sensor market, including radar, imagers, and spectroscopy. The research and development opportunities at device, packaging and system/algorithm levels are both challenging and exciting and technologies such as low-cost deep submicron CMOS, SiGe, and other compound materials are promising from different performance and figure of merit criteria. Many cases demand a hybrid integration as a system-in-package. This talk will cover some of the most important current and upcoming technologies and trade-offs for the millimeter-wave sensor market.

About Dr. Ahmad Bahai

Dr. Ahmad Bahai is a senior vice president and chief technology officer (CTO) of Texas Instruments responsible for guiding break-through innovation, corporate research and Kilby Labs. Throughout his career, Dr. Bahai has held a number of leadership roles, including director of research labs and chief technology officer of National Semiconductor, technical manager of a research group at Bell Laboratories, and founder of Algorex, a communication and acoustic IC and system company that was acquired by National Semiconductor. He holds an M.S. degree in Electrical Engineering from Imperial College, University of London and a Ph.D. in Electrical Engineering from the University of California, Berkeley. He is an IEEE Fellow; he was a professor in residence at UC Berkeley from 2001–2010; and he currently serves as an adjunct professor at Stanford University.

RFIC/IMS Joint Technical Lectures

Monday, 21 June 2021

12:30–14:00

Chair: Mona Hella, Rensselaer Polytechnic Institute

A Tour Through the World of Si IC Power Amplifiers

Speaker: **Peter Asbeck**, *Professor, University of California, San Diego, USA*

Abstract: While power amplifier design enjoys a rich history, it remains a vibrant and exciting area with many opportunities for innovation. This presentation reviews fundamentals of microwave and mm-wave power amplifier operation and implementation in Si ICs, and provides background to on-going research. Si technologies afford major leverage for power amplifiers, including very high f_t and f_{max}, excellent switches, vast integration opportunities for combination with LNAs, DACs and digital circuits, in addition to their cost advantage. They also pose challenges, stemming from limited voltage handling, conducting substrates, only modest carrier mobility, and thermal issues. The presentation highlights the ways in which advantages are exploited, and disadvantages are addressed. Power limits for Si transistors along with tradeoffs with f_t, will be discussed along with comparisons between SiGe HBT and CMOS (bulk planar, SOI, finFET and LDMOS). Cascode and stacking strategies will be reviewed and techniques for power combining will then be presented, with emphasis on application of transformers, and distinctions between single-ended and differential operation. The lecture will go over load pull and matching requirements, together with a quick review of harmonic matching considerations, amplifier classes, factors affecting efficiency, and basic reliability issues. Turning to the area of power amplifier architectures and design, the principles of switching-mode operation will be reviewed, and power DACs and switched capacitor power amplifiers will be discussed. Classical architectures for high backoff efficiency — envelope tracking, Doherty and outphasing — will be outlined, along with other load modulation approaches. Finally, application areas and representative IC examples will be discussed, including moderate power ICs in the microwave region, 5G-oriented mm-wave communications, and above 100GHz. The presentation concludes with a discussion of future areas of Si power amplifier research, including opportunities for covering wider frequency ranges, and adapting to different environmental conditions (such as VSWR) while maintaining high linearity (with the possible use digital or analog predistortion, including AI techniques). Possibilities for reaching "THz" frequencies (>300GHz) will also be described.

RFIC/IMS Joint Technical Lectures

Tuesday, 22 June 2021

12:00–13:30

Chair: Jeff Nanzer, Michigan State University

Micro-Motion Sensing Radar – Theory, System Architectures, and Circuit Implementations

Speaker: **Jenshan Lin**, *Professor, University of Florida, USA*

Abstract: Microwave radars have been used in many applications covering long distance (e.g., Doppler weather radar and airplane radar) to short distance (e.g., automobile radar and motion-sensing security radar). Stimulated by successful demonstrations of new system architectures and detection methods from many research groups in the 21st century, there have been growing interests of using short-range microwave radar techniques to detect small-scale motions or fine features of motions on humans and animals (e.g., heartbeat, respiration, acoustic vibration, finger gesture, gaits) for various applications (e.g., biology, medicine, security, emergency rescue, human-machine interface). As such radar techniques allow vast amount of body motion data to be collected for statistical analysis, biometric sensing becomes possible. This lecture will cover the fundamentals of micro-motion sensing radar. Different detection methods, system architectures, and circuit implementations will be discussed. The lecture will review key historical developments in this field. It will explain to audience why a very simple single-tone continuous wave (CW) radar can detect very small and very low-frequency cardiorespiratory body motions without being affected by the high $1/f$ noise in electronic circuits (e.g., in CMOS circuits). The lecture will also explain why it is very challenging to accurately separate heartbeat motion signals from respiration motion signals, and several methods proposed to overcome this challenge will be discussed. While the lecture will focus on hardware implementations, a few signal-processing algorithms will also be introduced. In addition, the speaker will comment on the applications and possible future developments.

RFIC/IMS Joint Technical Lectures

Wednesday, 23 June 2021

12:00–13:30

Chair: Jeff Nanzer, Michigan State University

Fully Integrated Terahertz Imaging and Spectroscopy: From Device to System

Speaker: **Ehsan Afshari**, *Professor, University of Michigan, USA*

Abstract: There is an increasing interest in low-cost mmWave and THz systems for imaging. Recent results in the lower THz frequencies (<1 THz) suggests that standard CMOS-BiCMOS processes can compete with compound semiconductors for some applications. In this lecture, we overview the application of THz imaging systems and their future for various markets. Next, we discuss major challenges in realizing these systems in CMOS. Moreover, we show several novel methods to overcome these challenges to realize complicated systems such as 2-D phased arrays for imaging and spectroscopy. The lecture has four major parts. First, motivations and applications of imaging and sensing will be reviewed. The lecture will then cover the fundamentals of device operation at high frequencies, and designs of basic circuit elements and major circuit building blocks at frequencies above 100 GHz. Finally, design and optimization of THz systems on chip will be discussed. The lecture is intended to enable RF circuit designers to implement circuits and systems at mmWave and THz frequencies through practical examples.

RFIC/IMS Joint Technical Lectures

Thursday, 24 June 2021

12:00–13:30

Chair: Jeff Nanzer, Michigan State University

mm-Wave "Wireless Fiber" to Meet the Capacity Demands of Future Networks

Speaker: **Amin Arbabian**, *Associate Professor, Stanford University, USA*

Abstract: Projections show the number of "Internet of Everything (IoE)" systems growing from the billions today to trillions by the next decade, largely fueled by the emergence of nodes that combine computation, communication, and sensing at the edge. This paradigm shift requires scalable backbone data pipelines to address the relentless growth in network traffic. To meet this challenge we need innovative approaches for the design of future systems both in the mobile link and for the backhaul. Millimeter-wave frequencies enable higher communication speeds due to the high spatial multiplexing degrees of freedom (DoF) as well as larger bandwidth available at mm-wave frequencies. Even in pure line-of-sight (LoS) environments, with reasonable array sizes, multi-stream parallelism can be attained leading to higher bounds for point-to-point mm-wave link capacity and achievable data rates. Towards this goal, this lecture covers spatial multiplexing over LoS multi-input multi-output (MIMO) systems as a vehicle to achieve Terabit-per-second wireless communication. The lecture will start by analyzing the challenges in silicon integration of scalable high-throughput mm-wave "Wireless Fiber" links. It will then cover tradeoffs in the partitioning of functionality between the transmitter and receiver, as well as between the analog and digital processing domains, and propose a scalable analog processing architecture for the receiver. An efficient transceiver architecture to address the main challenges for analog-based processing techniques enabling bandwidth-, range-, and size-scalable arrays for line-of-sight mm-wave communications is discussed. Finally, the experimental results for a 130 GHz wireless LoS MIMO transceiver, which uses fully packaged transmit and receive arrays and supports multiple independent broadband complex streams, is covered. Moving forward, this analog processing architecture provides a path to achieve robust data transmission at rates approaching 1 Tbps over distances that span tens of meters.

RFIC/IMS Joint Panel Session

Tuesday, 22 June 2021

12:30–14:00

Panel Sessions Chairs
RFIC: Jennifer Kitchen, Arizona State University
IMS: Ruonan Han, MIT
Rui Ma, MERL

RFIC Startups: A Dead Horse in the Era of Software Unicorns and Pandemics?

Panel Organizers and Moderators:
Oren Eliezer, *Ambiq*
Joseph Cali, *BAE Systems*
François Rivet, *University of Bordeaux*
Jacques C. Rudell, *University of Washington*
Jim Ahne, *Guerilla RF*

Panelists: **Amitava Das**, *Tagore Technology*
Joy Laskar, *Maja Systems*
Wouter Steyaert, *Tusk IC*
Tomi-Pekka Takalo, *CoreHW*
Harish Krishnaswamy, *MixComm*

Abstract: RFIC and microwave startups are not an easy job, especially when compared with many successful software startup companies that appeared to have effortlessly reached a high number of users without ever delivering a physical hardware product. Many of these companies have already exceeded billion-dollar valuation, thereby qualifying as a "unicorn".

In contrast, RFIC and microwave companies experience long and costly development and productization cycles, due to the high costs of the personnel, CAD tools, IC fabrication, measurement equipment, and marketing and delivery logistics, all of which have become particularly difficult under the Covid-19 social-distancing restrictions. What's more, nowadays these entrepreneurs face competition from the software unicorns for attention and funds of potential investors, as well as attracting young talent into the field.

In this lunchtime panel, several entrepreneurs at different levels of the maturity of their companies will share their experiences: how they were able to bootstrap the activity from a funding point of view, their business strategies to compete in a given market, and what challenges they have been facing. They will also discuss the uncertainties, as well as opportunities, that the pandemic brings about. The panel will try to answer questions such as whether the development of RFICs will soon be done only in the existing large companies and what the chances of success are for an RFIC startup.

Come and share your own experiences, opinions and questions!

RFIC Panel Session

Wednesday, 23 June 2021

12:30–14:00

Panel Sessions Chair: Jennifer Kitchen, Arizona State University

Automotive Radars and AI: Is My Car Really Safe?

Panel Organizers and Moderators:
François Rivet, *University of Bordeaux*
Magnus Wiklund, *Qualcomm*

Panelists: **Margaret Huang**, *Intel*
Karam Noujeim, *Anritsu*
Juergen Hasch, *Bosch*
Manju Hedge, *Uhnder*
Mohammad Emadi, *Zadar Labs*
Yue Lu, *DiDi Chuxing*

Abstract: Are we ready to take our hands off the car steering wheel? In any case, our cars are ready to steal control from us and remove the largest cause of road accidents: man. This panel will ask the question of how much confidence we have in the electronics of our cars and whether we can trust them. Automotive radar is the vision and artificial intelligence is the decision making. We will discuss the feasibility of this vision to determine if it is wise enough to stop driving or if we should keep our hands on the steering wheel.

RFIC Symposium Showcase

Sunday, 20 June 2021
10:00–12:00

RFIC Industry Showcase

Chair: Fred Lee, Twenty/Twenty Therapeutics

The RFIC Industry Showcase highlights eight outstanding industry papers, which are listed below. These papers received nominations for this recognition from the TPC sub-committees and godparents in a double-blind review. From these top eight papers, a two stage double-blind review process was conducted with a committee of eight judges selected from the TPC that did not have conflict of interest. Finally, the Best Paper Chair and other key Steering Committee members finalize the top three winners after rigorous reviews and discussions. The top three will be displayed on the RFIC website and on a rolling slideshow prior to the RFIC Plenary Session on 7 June 2021. Each winner will receive a plaque and will be recognized in an upcoming Microwave Magazine article. This year's Industry Paper Award finalists are:

Doubly-Tuned Transformer-Based Class-E Power Amplifiers in 130nm BiCMOS for mmWave Radar Sensors
Texas Instruments, USA
Tolga Dinc, Siraj Akhtar, Sachin Kalia, Baher Haroun, Swaminathan Sankaran
RTu1E-1

A High-Power SOI-CMOS PA Module with Fan-Out Wafer-Level Packaging for 2.4GHz Wi-Fi 6 Applications
[1]CEA-Leti, France, [2]Keysight Technologies, France, [3]Amkor Technology, Portugal
P. Reynier[1], A. Serhan[1], D. Parat[1], R. Mourot[1], M. Gaye[2], P. Kauv[2], A. Cardoso[3], A. Gouvea[3], S. Nogueira[3], A. Giry[1]
RTu1G-5

A 128Gb/s PAM4 Linear TIA with 12.6pA/√Hz Noise Density in 22nm FinFET CMOS
Intel, USA
Saeid Daneshgar, Hao Li, Taehwan Kim, Ganesh Balamurugan
RTu2G-2

An FBAR Driven -261dB FOM Fractional-N PLL
Broadcom, USA
Dihang Yang, David Murphy, Hooman Darabi, Arya Behzad, Richard Ruby, Reed Parker
RTu2H-1

A Sub-100fs JitterRMS, 20-GHz Fractional-N Analog PLL Using a BAW Resonator Based 2.5GHz On-Chip Reference in 22-nm FD-SOI Process
Texas Instruments, USA
Sachin Kalia, Salvatore Finocchiaro, Ashwin Raghunathan, Bichoy Bahr, Tolga Dinc, Gerd Schuppener, Siraj Akhtar, Tobias Fritz, Baher Haroun, Swaminathan Sankaran
RTu2H-2

A 24.5–29.5GHz Broadband Parallel-to-Series Combined Compact Doherty Power Amplifier in 28-nm Bulk CMOS for 5G Applications
Samsung, Korea
Seokhyeon Kim, Hyun-Chul Park, Daehyun Kang, Donggyu Minn, Sung-Gi Yang
RTu3E-3

A 5G FR2 (n257/n258/n261) Transmitter Front-End with a Temperature-Invariant Integrated Power Detector for Closed-Loop EIRP Control
[1]Samsung, USA, [2]Samsung, Korea
Chechun Kuo[1], Helen Zhang[1], Anirban Sarkar[1], Xiaohua Yu[1], Venumadhav Bhagavatula[1], Ashutosh Verma[1], Tienyu Chang[1], Ivan Siu-Chuang Lu[1], Daeyoung Yoon[2], Sangwon Son[1], Thomas Byunghak Cho[2]
RTu3E-4

A Fully-Digital 0.1-to-27Mb/s ULV 450MHz Transmitter with Sub-100μW Power Consumption for Body-Coupled Communication in 28nm FD-SOI CMOS
[1]STMicroelectronics, France, [2]IEMN (UMR 8520), France, [3]University of California, Berkeley, USA
Guillaume Tochou[1], Robin Benarrouch[1], David Gaidioz[1], Andreia Cathelin[1], Antoine Frappé[2], Andreas Kaiser[2], Jan Rabaey[3]
RTu3G-1

Industry Paper Contest Eligibility: The first author must have an affiliation from industry. The first author must also be the lead author of the paper and must submit a pre-recorded technical presentation to be shown during the virtual conference.

RFIC Symposium Showcase (continued)

Sunday, 20 June 2021

10:00–12:00

RFIC Student Paper Awards Finalists

Chair: Danilo Manstretta, Università di Pavia

The RFIC Symposium's Student Paper Award is devised to both encourage student paper submissions to the conference as well as give the authors of the finalists' papers a chance to promote their research work with the conference attendees with 3-minute videos during the RFIC Symposium Showcase. A total of thirteen outstanding student paper finalists were nominated this year by the RFIC Technical Program Committee to enter the final contest. A committee of ten TPC judges have selected the top-three papers after rigorous reviews and discussions. All finalists benefit from a complimentary RFIC registration. The top-three Student Papers be displayed on the RFIC website and on a rolling slideshow prior to the RFIC Plenary Session on 7 June 2021 in Atlanta. Each winner will receive an honorarium and a plaque. This year's Student Paper Award finalists are:

A Compact 196GHz FSK Transmitter for Point-to-Point Wireless Communication with Novel Direct Modulation Technique
Lili Chen[1], Samir Nooshabadi[2], Andreia Cathelin[3], Ehsan Afshari[1]
[1]University of Michigan, USA, [2]Caltech, USA, [3]STMicroelectronics, France
RTu1E-3

A 140GHz T/R Front-End Module in 22nm FD-SOI CMOS
Xinyan Tang, Johan Nguyen, Giovanni Mangraviti, Zhiwei Zong, Piet Wambacq
imec, Belgium
RTu1F-4

A 27.5dBm EIRP D-Band Transmitter Module on a Ceramic Interposer
Ali A. Farid, Ahmed S.H. Ahmed, Mark J.W. Rodwell
University of California, Santa Barbara, USA
RTu1G-1

A Frequency-and-Spatial Blocker Tolerant Butler Matrix Based 4×4 MIMO Receiver Using a Switched-Capacitor Quadrature Coupler
[1]GLOBALFOUNDRIES, India, [2]IIT Guwahati, India
Prateek Kumar Sharma[1], Nagarjuna Nallam[2]
RTu1H-1

A 3.7–6.5GHz 8-Phase N-Path Mixer-First Receiver with LO Overlap Suppression Achieving <5dB NF and >5dBm OOB B1dB
Shimin Huang, Alyosha Molnar
Cornell University, USA
RTu1H-3

A Global Multi-Standard/Multi-Band 17.1–52.4GHz Tx Phased Array Beamformer with 14.8dBm OP1dB Supporting 5G NR FR2 Bands with Multi-Gb/s 64-QAM for Massive MIMO Arrays
Abdulrahman A. Alhamed, Gabriel M. Rebeiz
University of California, San Diego, USA
RTu2E-1

A 130–151GHz 8-Way Power Amplifier with 16.8–17.5dBm Psat and 11.7–13.4% PAE Using CMOS 45nm RFSOI
Siwei Li, Gabriel M. Rebeiz
University of California, San Diego, USA
RTu2F-1

A Sub-0.25pJ/Bit 47.6-to-58.8Gb/s Reference-Less FD-Less Single-Loop PAM-4 Bang-Bang CDR with a Deliberately-Current-Mismatch Frequency Acquisition Technique in 28nm CMOS
Xiaoteng Zhao, Yong Chen, Lin Wang, Pui-In Mak, Franco Maloberti, Rui P. Martins
University of Macau, China
RTu2G-1

A 10.7–14.1GHz Reconfigurable Octacore DCO with -126dBc/Hz Phase Noise at 1MHz Offset in 28nm CMOS
Lorenzo Tomasin[1], Giovanni Boi[2], Fabio Padovan[2], Andrea Bevilacqua[1]
[1]Università di Padova, Italy, [2]Infineon Technologies, Austria
RTu3F-1

A mm-Wave Transmitter MIMO with Constellation Decomposition Array (CDA) for Keyless Physically Secured High-Throughput Links
Naga Sasikanth Mannem, Tzu-Yuan Huang, Elham Erfani, Sensen Li, Hua Wang
Georgia Tech, USA
RTu3G-2

A 0.31THz CMOS Uniform Circular Antenna Array Enabling Generation/Detection of Waves with Orbital-Angular Momentum
Muhammad Ibrahim Wasiq Khan[1], Jongchan Woo[1], Xiang Yi[1], Mohamed I. Ibrahim[1], Rabia Tugce Yazicigil[2], Anantha Chandrakasan[1], Ruonan Han[1]
[1]MIT, USA, [2]Boston University, USA
RTu3G-3

A 3.3–4.5GHz Fractional-N Sampling PLL with a Merged Constant Slope DTC and Sampling PD in 40nm CMOS
Gaofeng Jin[1], Fei Feng[1], Xiang Gao[1], Wen Chen[2], Yiyang Shu[2], Xun Luo[2]
[1]Zhejiang University, China, [2]UESTC, China
RTu4F-1

An Electrical Balance Duplexer for FDD Radios That Isolates TX from RX Independently in Two Bands
Kejian Shi[1], Hooman Darabi[2], Asad A. Abidi[1]
[1]University of California, Los Angeles, USA, [2]Broadcom, USA
RTu4G-1

Student Paper Contest Eligibility: The student must have been a full-time student (9 hours/term graduate, 12 hours/term undergraduate) during the time the work was performed. The student must also be the lead author of the paper and must present the paper at the Symposium.

RFIC Systems and Application Forum

Thursday, 24 June 2021

12:30–14:00

Chair: Oren Eliezer, Ambiq
Co-Chair: Travis Forbes, Sandia National Laboratories

The RFIC Systems and Application Forum is a demo session providing recorded demonstrations of the work reported in eight papers from various sessions of the RFIC Symposium. These will be accompanied by live online discussions with the authors, allowing attendees to meet the authors and learn more about their work, as well as to interact with other attendees of that session. The demo session includes both full systems incorporating more than one RFIC, as well as building-blocks/subsystems that are demonstrated with a system built around them (typically including test equipment). Below is a list of the authors who had volunteered to prepare demos for this session and the corresponding papers and oral presentation sessions.

Portable Thermoacoustic Imaging for Biometric Authentication Using a 37.3dBm Peak Psat 4.9GHz Power Amplifier in 55nm BiCMOS
[1]Stanford University, USA, [2]STMicroelectronics, France
Christopher Sutardja[1], Andreia Cathelin[2], Amin Arbabian[1]
RTu1E-2

A 27.5dBm EIRP D-Band Transmitter Module on a Ceramic Interposer
University of California, Santa Barbara, USA
Ali A. Farid, Ahmed S.H. Ahmed, Mark J.W. Rodwell
RTu1G-1

A 3.5-to-6.2-GHz Mixer-First Acoustic-Filtering Chipset with Mixed-Domain Asymmetric IF and Complex BB Recombination Achieving 170MHz BW and +27dBm IIP3 at 1×BW Offset
University of Illinois at Urbana-Champaign, USA
Hyungjoo Seo, Mengze Sha, Jin Zhou
RTu1H-2

A Noise-Cancelling Self-Interference Canceller with +7dBm Self-Interference Power Handling in 0.18μm CMOS
[1]Oregon State University, USA, [2]Columbia University, USA
Mostafa Essawy[1], Amin Aghighi[1], Hayden Bialek[1], Aravind Nagulu[2], H. Krishnaswamy[2], A. Natarajan[1]
RTu1H-5

A Global Multi-Standard/Multi-Band 17.1–52.4GHz Tx Phased Array Beamformer with 14.8dBm OP1dB Supporting 5G NR FR2 Bands with Multi-Gb/s 64-QAM for Massive MIMO Arrays
University of California, San Diego, USA
Abdulrahman A. Alhamed, Gabriel M. Rebeiz
RTu2E-1

A Fully-Digital 0.1-to-27Mb/s ULV 450MHz Transmitter with Sub-100µW Power Consumption for Body-Coupled Communication in 28nm FD-SOI CMOS

[1]STMicroelectronics, France, [2]IEMN (UMR 8520), France, [3]University of California, Berkeley, USA

Guillaume Tochou[1], Robin Benarrouch[1], David Gaidioz[1], Andreia Cathelin[1], Antoine Frappé[2], Andreas Kaiser[2], Jan Rabaey[3]

RTu3G-1

An 84.48Gb/s CMOS D-Band Multi-Channel TX System-in-Package

CEA-Leti, France

Abedelaziz Hamani, Francesco Foglia-Manzillo, Alexandre Siligaris, Nicolas Cassiau, Benjamin Blampey, Frederic Hameau, Cedric Dehos, Antonio Clemente, Jose Luis Gonzalez-Jimenez

RTu3G-4

A 4Rx, 4Tx Ka-Band Transceiver in 40nm Bulk CMOS Technology for Satellite Terminal Applications

[1]EnSilica, UK, [2]Satellite Applications Catapult, UK

Alan Chi-Wai Wong[1], Gabriele Devita[1], Shi-Ming Wu[1], Franco Lauria[1], Majd Eid[1], Omotade Illuromi[1], Samson Ogunkunle[1], Alessandro Modigliana[2]

RTu4E-1

Connected Future Summit (at IMS2021)

Wednesday, 23 June 2021
09:00–16:30

Chairs

Shahriar Shahramian, Nokia
Aida Vera Lopez, Intel
Clay Couey, Atlanta Micro

The wireless connectivity landscape is changing rapidly with the evolution of WiFi and the move to connect the unconnected via broadband wireless with low-Earth orbit (LEO) satellite constellations. The 5G standardization, deployment, and R&D of the next generations are impacting the future directions of connectivity in coordination with beyond-WiFi7 technologies, LEO satellite-based wireless networks, autonomous vehicle-to-everything communication.

Since its inception at IMS2017 in Honolulu, Hawaii, the 5G Summit has been held during Microwave Week. As 5G deployments are being planned, IMS2021 will host the Connected Future Summit, replacing the 5G Summit, to create a new platform for discussing various connectivity technologies and applications as well as the coexistence of different wireless standards to enable a safer and smarter world. The planned Connected Future Summit will review core technologies for future wireless networks.

09:00–09:40 "Connected Future with 5G and Beyond: Perspectives from 3GPP", **Richard Burbidge**, *Intel*

09:40–10:20 "Next Generation Wi-Fi: Wi-Fi 6/6E and Beyond", **Carlos Cordeiro**, *Intel*

10:20–11:00 "Communications in the 6G Era", **Harish Viswanathan**, *Nokia Bell Labs*

11:00–11:10 Break

11:10–11:50 "RF, mmWave and subTHz Semiconductor Trends & the Outlook Towards 6G", **Jon Strange**, *MediaTek*

11:50–12:30 "Test and Validation in the 6G Era: From DC to Daylight", **Roger Nichols**, *Keysight Technologies*

12:30–13:30 Lunch Break

13:30–14:10 "CoSOI and SiGe Technologies for mm-Wave Applications", **Ned Cahoon**, *GLOBALFOUNDRIES*

14:10–14:50 "Commercial mmW 5G with Scalable Active Antennas", **Nitin Jain**, *Anokiwave*

14:50–15:30 "OTA Test of Integrated mmWave Wireless Devices", **Kate Remley**, *NIST*

15:30–15:45 Break

15:45–16:30 Panel Discussions

Tuesday, 22 June 2021
10:00–11:40

Session RTu1E
Circuits and Systems for Microwave and mm-Wave Sensing, Radar and Communications
Chair: Gernot Hueber, Silicon Austria Labs, Austria
Co-Chair: Duane Howard, Amazon Web Services, USA

RTu1E-1
Doubly-Tuned Transformer-Based Class-E Power Amplifiers in 130nm BiCMOS for mmWave Radar Sensors

Tolga Dinc, Siraj Akhtar, Sachin Kalia, Baher Haroun, Swaminathan Sankaran; Texas Instruments, USA

Abstract: This paper presents high-efficiency V-band and E-band power amplifiers (PAs) for mmWave radar sensors. High-efficiency mmWave operation is enabled by a doubly-tuned transformer-based Class-E output network which allows increasing PA device size beyond the limit imposed by traditional Class-E principles, while preserving the Class-E voltage and current waveforms. Two primary prototypes (a 79-GHz centered two-stage PA and a 63-GHz centered single-stage PA) along with a 79 GHz single-stage test chip have been designed and fabricated in a production 130nm BiCMOS process. The two-stage PA also employs a Class-E driver stage with a split-and-combine 45-degree transformer to ease driving the large switching PA devices. The measurements results yield a peak PAE of 30.5/34.7% with an output power of 17/18.1dBm for the 79 GHz two-stage and single-stage 63 GHz PAs, respectively (along with a peak PAE of 32.6% at 17dBm for the 79 GHz single-stage test-chip). These are the best-in-class PAE numbers reported for V-Band and E-Band PAs in any silicon process, demonstrating the efficacy of the proposed doubly-tuned transformer-based Class-E network.

RTu1E-2
Portable Thermoacoustic Imaging for Biometric Authentication Using a 37.3dBm Peak P_{sat} 4.9GHz Power Amplifier in 55nm BiCMOS

Christopher Sutardja[1], Andreia Cathelin[2], Amin Arbabian[1]; [1]Stanford University, USA, [2]STMicroelectronics, France

Abstract: Handheld microwave thermoacoustic imaging (TA) can be used to image subcutaneous vasculature for biometric authentication and to monitor blood-vessel health, but the system requires a compact silicon microwave power amplifier (PA) with peak output power on the order of 10 W to be portable, affordable, and ubiquitous. This work presents a 55nm BiCMOS 4.9 GHz PA with 37.3 dBm peak output power that operates at a pulse width of 50 ns – 2 μs for a duty cycle of 0.025–1%. The PA serves as the transmitter in a microwave TA system, which generates the first known TA images of tissue phantoms using a compact transmitter built on a silicon substrate.

RTu1E-3

A Compact 196GHz FSK Transmitter for Point-to-Point Wireless Communication with Novel Direct Modulation Technique

Lili Chen[1], Samir Nooshabadi[2], Andreia Cathelin[3], Ehsan Afshari[1]; [1]University of Michigan, USA, [2]Caltech, USA, [3]STMicroelectronics, France

Abstract: A compact, fully-integrated 196GHz FSK transmitter for point-to-point wireless communication is prototyped with a 55nm SiGe BiCMOS process, demonstrating a single-channel data rate of 10Gb/s with a chip area of 0.68mm^2. The achieved single-channel data rate is around 5× higher compared with all other FSK wireless transmitters and the chip area is around 4× smaller compared with other state-of-the-art sub-THz wireless transmitters. Unlike conventional FSK transmitters which encode data with two oscillators at different frequencies or with the control voltage of varactors in the LC tank, the proposed FSK transmitter performs data modulation by varying the phase shift of tunable phase shifting couplers in a coupled oscillator loop, resolving the issues of extra power consumption and long frequency settling time. In theory, frequency shift based on this mechanism is instantaneous without overshoot/undershoot issues.

RTu1E-4

A 135–155GHz 9.7%/16.6% DC-RF/DC-EIRP Efficiency Frequency Multiply-by-9 FMCW Transmitter in 28nm CMOS

Sehoon Park, Dae-Woong Park, Kristof Vaesen, Anirudh Kankuppe, Barend van Liempd, Piet Wambacq, Jan Craninckx; imec, Belgium

Abstract: A low-power and high efficiency 135–155 GHz FMCW radar transmitter (TX) in 28 nm CMOS is presented. Starting from a 16 GHz signal, the ×9 frequency multiplier chain proposes phase-controlled frequency triplers at D-band and V-band exploiting phase aligned harmonic generation for high efficiency, conversion gain and output power, avoiding the use of power-hungry buffer stages. The PA proposes a wideband maximum achievable gain (G_{max}) core to mitigate the gain limitation of D-band amplifiers. The design integrates an on-chip antenna and an optimized PA to antenna interface. The TX achieves a EIRP of 9.4 dBm with 9.7%/16.6% DC-RF/DC-EIRP efficiency which is the highest among the state-of-the-art D-band frequency multiplier chains multiplying more than four.

RTu1E-5

A Low Power 35GHz HEMT Oscillator for Electron Spin Resonance Spectroscopy

Nergiz Sahin-Solmaz, Alessandro V. Matheoud, Giovanni Boero; EPFL, Switzerland

Abstract: This paper presents a low power microwave oscillator designed as sensor for electron spin resonance (ESR) spectroscopy. Low power consumption is necessary for low temperature operation. Additionally, lower power consumption allows for a lower microwave magnetic field in the sensing volume, which avoids the saturation of samples having long spin relaxation times and, consequently, the degradation of the spin sensitivity. The oscillator operates at 35 GHz, consuming 90 μW at 300 K and 15 μW at 1.4 K. This is the lowest power consumption reported to date for oscillators operating in the same frequency range. The fully integrated oscillator is based on a single HEMT transistor having a gate length of 70 nm and realized using a 2DEG in $In_{0.7}Ga_{0.3}As$. The chip area is about 0.3 mm^2. The spin sensitivity is 3×10^8 spins/$Hz^{1/2}$ at 300 K and 1.2×10^7 spins/$Hz^{1/2}$ at 10 K.

Tuesday, 22 June 2021
10:00–11:40

Session RTu1F
High Performance mm-Wave Front-End Circuits
Chair: Kamran Entesari, Texas A&M University, USA
Co-Chair: Domine M.W. Leenaerts, NXP Semiconductors, The Netherlands

RTu1F-1
A 39GHz T/R Front-End Module Achieving 25.6% PAE_{max}, 20dBm P_{sat}, 5.7dB NF, and -13dBm IIP3 in 22nm FD-SOI for 5G Communications

Zhiwei Zong[1], Johan Nguyen[1], Yao Liu[2], Yang Zhang[2], Xinyan Tang[1], Giovanni Mangraviti[2], Piet Wambacq[1]; [1]Vrije Universiteit Brussel, Belgium, [2]imec, Belgium

Abstract: This paper presents a 39 GHz front-end module (FEM) in 22 nm FD-SOI technology for 5G communications. The PA output stage uses a 2-stacked FET topology to achieve high output power. A two-way current combiner is used to combine output power from the output stage while maintaining a uniform waveform distribution over each transistor unit cell to enhance the device reliability. The LNA consists of two stages to obtain high power gain with low power consumption. Derivative-superposition (DS) with a common-mode inductor is used to improve the LNA linearity. The measured P_{sat} and PAE_{max} in TX mode are 20.4 dBm and 25.6%, respectively. The measured NF and IIP3 in RX mode are 5.7 dB and -13 dBm, respectively. A $P_{out,avg}$ of 13.5 dBm and a PAE_{avg} of 10.6% is achieved in 64-QAM 400 MSym/s single-carrier at EVM_{rms} of -25 dB for TX-mode.

RTu1F-2
A 22.2–43GHz Gate-Drain Mutually Induced Feedback Low Noise Amplifier in 28-nm CMOS

Ali Ershadi, Samuel Palermo, Kamran Entesari; Texas A&M University, USA

Abstract: A novel mm-wave low-noise-amplifier (LNA) architecture capable of achieving simultaneous power and noise matching over a large bandwidth is proposed. It is shown that by magnetically coupling a pair of inductors connected at the gate and drain of a transistor, a loss-less (series-series) feedback path from the drain-current to the gate is generated which: 1) Increases the transistor input impedance magnitude, 2) generates a real-impedance part which can be controlled for power-matching, and 3) brings the optimum noise source impedance close to the optimum power matching impedance. The prototype is fabricated in TSMC 28-nm bulk CMOS process. The measured chip is functional from 22.2 to 43 GHz, while providing 21 dB of peak gain, minimum NF of 3.5 dB, and an average IIP_3 of -3 dBm.

RTu1F-3

A Millimeter-Wave LNA in 45nm CMOS SOI with Over 23dB Peak Gain and Sub-3dB NF for Different 5G Operating Bands and Improved Dynamic Range

Sensen Li[1], Tzu-Yuan Huang[1], Yuqi Liu[1], Hyunjin Yoo[2], Yoosam Na[2], Youngsik Hur[2], Hua Wang[1]; [1]Georgia Tech, USA, [2]Samsung, Korea

Abstract: This paper presents a variable gain CMOS low-noise amplifier (LNA) with high gain and low noise figure, aiming at 5G communication. The LNA is based on a 3-stage inductively degenerated amplifier with the first stage as common-source amplifier for optimized overall noise performance, and the following two stages as cascode amplifiers for a higher gain and reverse isolation. Variable gain control with an amplification-bypass mode is implemented, facilitating the LNA/receiver to cope with the significantly different power level and thus maximizing its operation dynamic range. Two designs are implemented following the same principle, with one covering N257/258 band and the other one targeting N260 band. Both designs achieve over 23dB peak power gain with below 3dB noise figure. Variable gain control is demonstrated with more than 15dB gain tuning range over frequencies. The LNA linearity is also characterized in measurement, showing an in-band IIP3 of -9.3dBm at 24.25GHz (N257/258 LNA) and -12.9dBm at 40GHz (N260 LNA).

RTu1F-4

A 140GHz T/R Front-End Module in 22nm FD-SOI CMOS

Xinyan Tang, Johan Nguyen, Giovanni Mangraviti, Zhiwei Zong, Piet Wambacq; imec, Belgium

Abstract: This paper presents a D-band front-end module (FEM) with an integrated transmit/receive (T/R) switch in 22-nm fully-depleted silicon on insulator (FD-SOI) CMOS technology for beyond-5G communication. The asymmetric T/R switch topology with intrinsic ESD protection leverages the Tx- and Rx-mode RF performance. Both the PA and LNA have a differential topology with transformer-based matching networks to eliminate unwanted effects from common-mode parasitics, especially at the antenna port. The adopted stacked-FET PA achieves a high output power while consuming much less area than a PA based on passive power combining. At 140 GHz, the Tx achieves a power gain G_p of 33.6 / 35.7 dB, a saturated output power Psat of 12.5 / 14.7 dBm, a peak power-added efficiency PAE of 10.8 / 11.3%, and output 1-dB compression point (OP1dB) of 9.4 / 11.2 dBm with nominal / boosted supplies. At 140 GHz, the Rx achieves a 20-dB G_p, a -24-dBm input 1-dB compression point (IP1dB), and a 9.2-dB noise figure (NF) with only 20-mW power consumption from a 0.8-V supply. This compact FEM has a PA / LNA core area of 0.024 / 0.032 mm^2, respectively.

RTu1F-5

A 10–110GHz LNA with 19–25.5dB Gain and 4.8–5.3dB NF for Ultra-Wideband Applications in 90nm SiGe HBT Technology

Oguz Kazan, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a broadband differential low-noise amplifier (LNA) at 10–110 GHz. The four-stage LNA is realized using 90 nm SiGe BiCMOS process having a 300 GHz f_T HBT. Resistive feedback is used for operation at 10–50 GHz, and a wideband collector load with a linear impedance increase versus frequency compensates for the transistor output capacitance and guarantees a monotonic increase in the gain from 60 to 100 GHz. The LNA has a measured small-signal gain of 19–25.5 dB and the measured noise figure (NF) is 4.8–5.3 dB at 10–50 GHz. The LNA also achieves an output-referred 1dB compression point (OP1dB) of -3.3 dBm at 66 GHz. The differential LNA consumes 96 mW (48 mW half circuit) with an active circuit area of 1.3×0.6 mm^2. Application areas are in wideband receivers and in wideband microwave and millimeter-wave instrumentation systems.

Tuesday, 22 June 2021
10:00–11:40

Session RTu1G
Advanced Techniques for Power Amplifier Modules, Sub-THz and BIST
Chair: Alvin Joseph, GLOBALFOUNDRIES, USA
Co-Chair: Fred Lee, Twenty/Twenty Therapeutics, USA

RTu1G-1
A 27.5dBm EIRP D-Band Transmitter Module on a Ceramic Interposer
Ali A. Farid, Ahmed S.H. Ahmed, Mark J.W. Rodwell; University of California, Santa Barbara, USA

Abstract: We present a fully packaged D-band direct conversion transmitter module on a low-permittivity ceramic carrier (Kyocera GL771, $\varepsilon_r = 5.2$, $\delta = 0.003$). The module has a broadband 135GHz 22FDX CMOS direct conversion transmitter, a medium-power (100mW P_{sat}) high-efficiency power amplifier implemented in Teledyne 250nm InP HBT technology, and a series-fed microstrip patch antenna array. The CMOS IC is flip-chip bonded to the carrier using 50 μm diameter copper studs, while the InP IC is wire bonded, with impedance-matching networks on the carrier compensating for the wire bonds' parasitic impedances. The module has 6GHz 3-dB modulation bandwidth and 27.5dBm measured effective isotropic radiated power (EIRP) at saturation. Under 5Gbaud, 64QAM modulation (30Gbps), the module shows 8.5% RMS error vector magnitude (EVM) at 21.5dBm EIRP. To our knowledge, the module has the highest reported EIRP and efficiency among D-band single channel transmitters.

RTu1G-2
305–325GHz Non-Reciprocal Isolator Based on Peak-Control Gain-Boosting Magnetless Non-Reciprocal Metamaterials
Yunfan Wang[1], Wenhua Chen[1], Xingcun Li[1], Shuyang Li[1], Peigen Zhou[2]; [1]Tsinghua University, China, [2]Southeast University, China

Abstract: Terahertz (THz) non-reciprocal components such as circulators, isolators, filters, and gyrators are anticipated to play vital roles in THz system. However, to the best of our knowledge, silicon-based THz non-reciprocal components have not been reported. This paper presents the first silicon-based THz magnetic-free non-reciprocal isolator in SiGe BiCMOS process (f_T/f_{max}=300/450 GHz), covering 305–325 GHz. Peak-control gain-boosting technique is utilized to push the operating frequency of the magnetless non-reciprocal metamaterials (MNMs) to THz spectrum. By cascading three MNMs operating at different frequencies, a wideband non-reciprocal isolator is achieved. It exhibits 3.6 dB loss (with pad) and 15.3 dB isolation while consuming 3.52 mW (1.17 mW/unit) from 0.88-V supply.

RTu1G-3

300–335GHz Highly Efficient Beam-Steerable Radiator Based on Tunable Boundary Conditions

Yunfan Wang, Wenhua Chen, Xingcun Li, Jiaxian Chen, Long Chen, Shuyang Li; Tsinghua University, China

Abstract: This paper presents a 299.4 GHz–335 GHz highly efficient beam-steerable radiator based on tunable boundary conditions. By controlling the states of switches, the equivalent boundary condition for the radiator is changed, enabling beam steering. The output of the harmonic voltage control oscillator (VCO) is boosted through two-dimensional harmonic boosting technique. The radiator is implemented in 130-nm SiGe BiCMOS process. It enables 20° scan ranges in the E-plane and 28° scan ranges in the H-plane. With/without lens, it achieves an equivalent isotropic radiated power (EIRP) of 20.8 dBm/2.4 dBm, 0.8 dBm/-2.6 dBm radiation power, 2.24%/1.02% DC-to-RF efficiency, and a competitive tuning-range of 11.2% for 1.7 V supply.

RTu1G-4

Sequential Loopback Built-In Self-Test Algorithm for Dual-Polarization Millimeter-Wave Phased-Array Transceivers

Seunguk Choi[1], Yuuichi Aoki[2], Hyun-Chul Park[2], Sung-Gi Yang[2], Ho-Jin Song[1]; [1]POSTECH, Korea, [2]Samsung, Korea

Abstract: This paper presents a built-in self-test (BIST) algorithm for dual-polarization millimeter-wave beamforming transceivers. The proposed algorithm provides simplified loopback paths that can be implemented with short and equi length interconnections between neighboring transmitters and receivers. End-to-end channel response measurements for all neighboring loopback paths enable us to extract the all relative complex channel responses to a reference channel. Verification of the proposed algorithm was conducted in a test setup with the 5G millimeter-wave communications chipset boards. Compared to the reference 1-by-1 measurements, the measured gain and phase rms errors of the proposed scheme were 0.4 dB, 2.8° for the Tx and 0.6 dB, 3.9° for the Rx. After the calibration, large phase deviation between channels were successfully reduced from 15.2° and 42.1° to 4.9° and 4.4° for the Tx and Rx, respectively, which is comparable to the accuracy limit due to the on-chip phase shifters.

RTu1G-5

A High-Power SOI-CMOS PA Module with Fan-Out Wafer-Level Packaging for 2.4GHz Wi-Fi 6 Applications

P. Reynier[1], A. Serhan[1], D. Parat[1], R. Mourot[1], M. Gaye[2], P. Kauv[2], A. Cardoso[3], A. Gouvea[3], S. Nogueira[3], A. Giry[1]; [1]CEA-Leti, France, [2]Keysight Technologies, France, [3]Amkor Technology, Portugal

Abstract: This paper presents the first high-power SOI-CMOS power amplifier (PA) embedded in a Fan-Out Wafer Level Package (FOWLP) and addressing 2.4 GHz Wi-Fi 6 applications. At 2.44 GHz, the PA delivers 35.1 dBm of saturated output power (P_{sat}) with 53% of peak PAE and 29.5 dB of power gain. Without DPD, the PA achieves state-of-the art measured performance with 26.5/24.5/21.9 dBm of linear output power (P_{out}) for an EVM (Error Vector Magnitude) of -30/-35/-43 dB with an operating current of 336/270/210 mA for MCS7/9/11 40MHz signals respectively. The PA shows robust operation under extreme load mismatch (8:1 VSWR) and temperature (-40 to 80°C) conditions.

Tuesday, 22 June 2021
10:00–11:20

Session RTu4F
High-Performance Fractional-N PLLs and Building Blocks
Chair: Joseph Cali, BAE Systems, USA
Co-Chair: Howard C. Luong, HKUST, China

RTu4F-1
A 3.3–4.5GHz Fractional-N Sampling PLL with a Merged Constant Slope DTC and Sampling PD in 40nm CMOS

Gaofeng Jin[1], Fei Feng[1], Xiang Gao[1], Wen Chen[2], Yiyang Shu[2], Xun Luo[2]; [1]Zhejiang University, China, [2]UESTC, China

Abstract: In this work, we present a novel fractional-N sampling PLL architecture where the functions of a constant slope digital-to-time converter (CS-DTC) and a sampling phase detector (SPD) are merged into one block. This simplifies the PLL's critical phase detection path, saves power, reduces noise sources and improves the overall linearity. The 3.3–4.5GHz PLL implemented in 40nm CMOS achieves a 292fs rms jitter, integrated from 10kHz to 10MHz while consuming 2.4mW, leading to a PLL FoM of -246.9dB. The in-band fractional spur is -54dBc and the PLL occupies a core area of 0.36mm^2.

RTu4F-2
A 18.9–22.3GHz Dual-Core Digital PLL with On-Chip Power Combination for Phase Noise and Power Scalability

Saleh Karman, Francesco Tesolin, Alessandro Dago, Mario Mercandelli, Carlo Samori, Salvatore Levantino; Politecnico di Milano, Italy

Abstract: This work presents a novel architecture of frequency synthesizer which allows to easily couple two digital PLLs (synchronized to the same reference source) and scale phase noise and power consumption. The second-harmonic component of the two digital oscillators are inductively extracted and power-combined on-chip. A digital correction loop guarantees phase alignment of the two PLLs even in the presence of mismatch. The frequency synthesizer spans from 18.8 to 22.3GHz, the phase noise at 1MHz offset scales from -113 to -116dBc/Hz and power consumption from 18.5 to 37.1mW, by activating one or two cores, respectively.

RTu4F-3

A 2.3–3.9GHz Fractional-N Frequency Synthesizer with Charge Pump and TDC Calibration for Reduced Reference and Fractional Spurs

Junning Jiang, Tanwei Yan, Dadian Zhou, Aydin Ilker Karsilayan, Jose Silva-Martinez; Texas A&M University, USA

Abstract: A 2.3–3.9 GHz fractional-N phase locked loop (PLL) with charge pump and a time-to-digital converter (TDC) based calibration for reference and fractional spurs reduction suitable for frequency synthesizers used in 5G mobile communication systems is introduced in this paper. The charge pump PLL includes a digital phase processor composed by a TDC, digital filters and a DTC and it is used for monitoring, tracking, and filtering both reference and fractional spurs simultaneously. Calibrated sub-ranging TDCs and DTC with 1 ps resolution are employed. A non-invasive master-slave calibration methodology is applied to TDCs and DTC with Vernier delay line structure to achieve the required INL and DNL performances. Fabricated in a mainstream 40-nm technology, the PLL is characterized, showing a reference spur level of -108.3 dBc and a fractional spur under -95.0 dBc. The frequency synthesizer's total power consumption when operating at 3.3 GHz is 15.7 mW.

RTu4F-4

A PVT-Compensated 0.1–67GHz Injection-Locked Frequency Divider with Replica-Based Automatic Tuning

Maarten Baert, Wim Dehaene; KU Leuven, Belgium

Abstract: This paper presents a PVT-tolerant wideband injection-locked frequency divider with a 0.1 GHz to 67 GHz frequency range, implemented in 28nm CMOS. The design uses complementary injection to achieve a wider locking range and a supply-based PVT-compensation to drastically reduce PVT sensitivity. A replica-based automatic tuning scheme is introduced to achieve a very wide frequency range without the need for manual tuning, while also increasing the sensitivity and minimizing the additive jitter. The resulting design achieves a locking range of 199.4% and an additive jitter of just 17 fs at an input frequency of 30 GHz.

Wednesday, 23 June 2021
10:00–11:40

Session RTu1H
Advanced N-Path Techniques and Associated Interference Mitigation
Chair: Alyosha Molnar, Cornell University, USA
Co-Chair: François Rivet, University of Bordeaux, France

RTu1H-1
A Frequency-and-Spatial Blocker Tolerant Butler Matrix Based 4×4 MIMO Receiver Using a Switched-Capacitor Quadrature Coupler

Prateek Kumar Sharma[1], Nagarjuna Nallam[2]; [1]GLOBALFOUNDRIES, India, [2]IIT Guwahati, India

Abstract: Recent advances in passive mixer-first receivers enhanced the frequency-blocker tolerance of radio-frequency (RF) receivers. These mixer-first receiver architectures are also extended to Multi-Input Single-Output (MISO) receivers. The current state-of-art Multi-Input Multi-Output (MIMO) receivers still use a low-noise amplifier (LNA) as the first block, thus have low frequency-blocker tolerance. This paper presents a Butler-matrix based 4×4 beamforming MIMO receiver with high frequency-and-spatial blocker tolerance using a novel switched-capacitor quadrature coupler. Other advantages of this RF LNA-less MIMO architecture include reduced power consumption, reduced active area, and improved in-band linearity. Measurement results of a CMOS prototype 4×4 MIMO receiver are presented. The prototype MIMO has a single-element P1dB of -9.6 dBm and an in-band/in-notch B1dB of -4 dBm at 0.8 GHz.

RTu1H-2
A 3.5-to-6.2-GHz Mixer-First Acoustic-Filtering Chipset with Mixed-Domain Asymmetric IF and Complex BB Recombination Achieving 170MHz BW and +27dBm IIP3 at 1×BW Offset

Hyungjoo Seo, Mengze Sha, Jin Zhou; University of Illinois at Urbana-Champaign, USA

Abstract: This paper presents a 3.5-to-6.2-GHz high-linearity mixer-first superheterodyne receiver chipset that utilizes gigahertz intermediate-frequency (IF) acoustic filters and a Weaver-like mixed-domain recombination architecture. The proposed mixed-domain recombination architecture enables a high IF (2.6 GHz) with a wide (170 MHz) instantaneous bandwidth (BW) and reduces the number of IF lossy passive components. Leveraging inherent quadrature down-conversion in the IF receiver, we adopt complex baseband signal processing to compensate in-phase and quadrature mismatch. Also, we identify that the IF integrated transformer loss is asymmetrical with respect to primary and secondary winding quality factors, and hence utilize stacked transformers for low loss and compact size. The chipset is fabricated using a 65-nm CMOS process and demonstrates, in measurement, an out-of-band IIP3 of +27 dBm at 1×BW offset with a 9.7-dB NF at 3.5-GHz RF.

RTu1H-3

A 3.7–6.5GHz 8-Phase N-Path Mixer-First Receiver with LO Overlap Suppression Achieving <5dB NF and >5dBm OOB B1dB

Shimin Huang, Alyosha Molnar; Cornell University, USA

Abstract: This paper presents an 8-phase N-path mixer-first receiver in 45nm SOI operating from 3.7–6.5GHz. The receiver implements an LO overlap suppression technique to relax the LO duty-cycle requirement for such mixers, allowing 8-phase 25% duty-cycle LO to realize 8-phase operation at higher frequencies. The prototype receiver achieves a noise figure of 2.4–4.7dB while consuming 89–135mW. The out-of-band (OOB) blocker 1dB compression point (B1dB) is >5dBm and OOB IIP3 is >+28dBm. The receiver allows 22–43dB third-order harmonic rejection (HR3) without any calibration, and up to 72dB HR3 with proper recombination weighting in DSP.

RTu1H-4

A Widely Tunable N-Path Frequency-Selective Limiter for Self-Adaptive Interference Suppression

Loai G. Salem; University of California, Santa Barbara, USA

Abstract: This paper reports the first widely tunable N-path frequency-selective limiter (FSL). Eight stagger-tuned 4-path filters are alternately summed to establish a 4-channel BPF with a steep roll-off between the passband and the stopband. The limiting action of an FSL is realized by autonomously modulating the frequency separation between each of the two 4-path filters within a channel to control the channel's passband gain. For input signals below -2 dBm, the FSL behaves as a conventional BPF with a 250 MHz bandwidth. At each input spectral component exceeding this limiting threshold, the FSL provides a variable notch in its passband with increasing attenuation of -10 dB for each +10-dB increase in the input component power to maintain the troubling tone output power below -1.3 dBm. The implemented 4-channel FSL using 0.18-μm CMOS is tunable from 0.3 GHz to 1 GHz and achieves a NF of 14.5 dB.

RTu1H-5

A Noise-Cancelling Self-Interference Canceller with +7dBm Self-Interference Power Handling in 0.18μm CMOS

Mostafa Essawy[1], Amin Aghighi[1], Hayden Bialek[1], Aravind Nagulu[2], H. Krishnaswamy[2], A. Natarajan[1]; [1]Oregon State University, USA, [2]Columbia University, USA

Abstract: Self-interference (SI) mitigation is critical for full-duplex and frequency-domain duplex systems. Canceller noise and linearity limits the SI power that can be tolerated at RX input. A dual-path SI cancellation scheme is presented where the noise and distortion from the canceller are addressed through a differential noise-cancelling path. The proposed scheme relaxes the noise/linearity trade-offs in canceller design and a 400MHz implementation in 0.18μm CMOS demonstrates 20 dB SI cancellation over 50MHz bandwidth and 23 dB cancellation for +1dBm peak SI power while degrading RX NF by 3.8 dB.

Wednesday, 23 June 2021
10:00–11:40

Session RTu2E
mm-Wave Circuits for 5G Systems
Chair: Jane Gu, University of California, Davis, USA
Co-Chair: Arun Natarajan, Oregon State University, USA

RTu2E-1
A Global Multi-Standard/Multi-Band 17.1–52.4GHz Tx Phased Array Beamformer with 14.8dBm OP1dB Supporting 5G NR FR2 Bands with Multi-Gb/s 64-QAM for Massive MIMO Arrays

Abdulrahman A. Alhamed, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a 4-channel 17.1–52.4 GHz (101.5% fractional bandwidth) Tx phased array front-end designed in SiGe BiCMOS SBC18S5 process. A wideband RF beamforming architecture employing 2-stage resistive-feedback power amplifier and active phase shiftier with T-coil wideband matching network results in an ultra wideband operation with high output power. Each channel has a 5-bit phase control and 15 dB gain control. The input signal is distributed to the 4 channels using a two-stage wideband compact Wilkinson network. The measured gain is 22 dB with 12–14.8 dBm OP1dB at 17–52 GHz. Each channel consumes 240–250 mW at P1dB from 2 and 3 V voltage supplies. The chip is tested with a 28 GHz 64-QAM signals and achieved a data-rate of 6Gb/s at -25 dBm EVM and 9.5 dBm average output power. To author's knowledge, this work achieves the widest bandwidth beamformer covering 5G NR FR2 bands and enabling the construction of multi-standard wideband phased arrays.

RTu2E-2
A High-Linearity, 24–30GHz RF, Beamforming and Frequency-Conversion IC for Scalable 5G Phased Arrays

Arun Paidimarri[1], Masayuki Yoshiyama[2], Jean-Olivier Plouchart[1], Alberto Valdes-Garcia[1], Wooram Lee[1], Yuma Okuyama[2], Mark Yeck[1], Caglar Ozdag[1], Sudipto Chakraborty[1], Yo Yamaguchi[2], Bodhisatwa Sadhu[1]; [1]IBM T.J. Watson Research Center, USA, [2]Fujikura, Japan

Abstract: Phased array antenna modules can benefit from splitting beamforming and frequency-conversion functions between different ICs to enable scalability, configurability and Si area efficiency. This work introduces a frequency-conversion IC that features architecture and high-linearity features that enable support of dual-polarized 5G scaled phased arrays with >64 antenna elements. The IC integrates two TX+RX frequency conversion cores (one for each antenna polarization). Each core comprises (1) an RX path with two high-linearity mixers sharing a common load for power combining, (2) a TX path with an up-conversion mixer followed by a power splitter and two PAs, and

(3) T/R switches. The IC occupies 10.6 mm^2 and supports 24–30 GHz RF and 2–5 GHz IF. On-wafer measurement results from the full IC and an RX mixer core breakout are presented. The TX path achieves 7–14 dBm oP1dB while the RX mixer achieves >+14 dBm IIP3 at 28GHz. The TX path has a conversion gain >25 dB and <12.5 dB NF. The RX path for a single-input has >-1 dB conversion gain and <15 dB NF.

RTu2E-3

A 17.3-mW 0.46-mm^2 26/28/39GHz Phased-Array Receiver Front-End with an I/Q-Current-Shared Active Phase Shifter for 5G User Equipment

Xiaohua Yu[1], Ajaypat Jain[1], Amitoj Singh[1], Omar Elsayed[1], Chechun Kuo[1], Hariharan Nagarajan[1], Daeyoung Yoon[2], Venumadhav Bhagavatula[1], Ivan Siu-Chuang Lu[1], Sangwon Son[1], Thomas Byunghak Cho[2]; [1]Samsung, USA, [2]Samsung, Korea

Abstract: This paper presents a 26/28/39GHz millimeter-wave phased-array receiver front-end (RXFE) including two parallel paths combined at the output. Each path consists of a T/R switch, a large dynamic range low noise amplifier (LNA), and an I/Q-current-shared active phase shifter. The RXFE achieves minimum NF of 4.3dB/5.6dB, maximum IP1dB of 0dBm/-1.3dBm, and best EVM of -33.1dB/-29.6dB for 26/28GHz band and 39GHz band, respectively, while consuming power of 17.3mW with 1.1V supply. The chip was fabricated in 28nm CMOS FD-SOI process and the RXFE occupied an area of 0.46mm^2 per channel.

RTu2E-4

A 28GHz Optically Synchronized CMOS Phased Array with an Integrated Photodetector

Matan Gal-Katziri, Craig Ives, Armina Khakpour, Ali Hajimiri; Caltech, USA

Abstract: This paper presents a modular 28 GHz phased array. Each of its 2×4-modules is driven by a CMOS RFIC, whose RF output is optically synchronized using a fully integrated silicon photodiode. The photocurrent is amplified using a tuned injection-locked TIA to serve as the reference for an on-chip synthesizer, which generates and distributes the RF signal to the PAs that drive the antennas. We demonstrate beam steering, data transmission, and synchronization of array modules up to 25m away from the clock source.

Wednesday, 23 June 2021
10:00–11:20

Session RTu2F
mm-Wave and Sub-THz Power Amplifiers
Chair: Steven Callender, Intel, USA
Co-Chair: Margaret Szymanowski, Crane Aerospace & Electronics, USA

RTu2F-1
A 130–151GHz 8-Way Power Amplifier with 16.8–17.5dBm Psat and 11.7–13.4% PAE Using CMOS 45nm RFSOI

Siwei Li, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a D-band linear power amplifier (PA) with high gain, high output power and high efficiency using CMOS 45nm RFSOI process. An 8-way (4-way differential) power-combining technique is implemented to increase the power amplifier linearity and output power. To decrease the loss of the output combiner, the first stage output power combiner is designed as part of the power matching network. The PA achieves a small-signal gain of 22.2–24 dB with 1–1.2 V supply at 140 GHz, respectively. The measured P1dB and Psat are 14.2 dBm and 17.5 dBm with 1.2 V supply, at 140 GHz. The maximum PAE is 13.4%. The 140 GHz PA operates from 130 to 150 GHz with an OP1dB > 13 dBm, which is ideal for high-speed wireless communication systems.

RTu2F-2
One Stage Gain Boosted Power Driver at 184GHz in 28nm FD-SOI CMOS

Sébastien Sadlo[1], Magali De Matos[2], Andreia Cathelin[1], Nathalie Deltimple[2]; [1]STMicroelectronics, France, [2]IMS (UMR 5218), France

Abstract: In order to improve amplifiers' power gain for a close to f_{max} operation, a methodology to size the embedding of any active two port is described and then applied to the design of a single-stage amplifier as a proof of concept. The 184 GHz measured 28 nm FD-SOI CMOS amplifier presents a power gain of 7.6 dB, a bandwidth of 20 GHz, a P_{sat} of -3.7 dBm and a peak PAE of 4.2% for a power consumption of 5.1 mW.

RTu2F-3

A Compact H-Band Power Amplifier with High Output Power

Ahmed S.H. Ahmed[1], Utku Soylu[2], Munkyo Seo[3], Miguel Urteaga[4], Mark J.W. Rodwell[2]; [1]Marki Microwave, USA, [2]University of California, Santa Barbara, USA, [3]Sungkyunkwan University, Korea, [4]Teledyne Scientific & Imaging, USA

Abstract: We report a compact H-band power amplifier with high output power in 250nm InP HBT technology. Stacking and parallel power combining together provide the desired output power. Common-base stages with base capacitive degeneration act as stacked power cells. Four power cells are combined by a compact low-loss 4:1 transmission line network. At 270GHz, the four-stage amplifier has 16.8dBm saturated output power with 4% power-added efficiency (PAE). Over 266–285GHz, the amplifier's saturated output power is 14–16.7dBm with an associated 2.2–4%PAE. The 3-dB small-signal bandwidth extends from 233GHz to 281GHz with a peak gain of 20.5dB at 264GHz. The amplifier has a compact area of 1.08mm×0.77mm and P_{sat}/mm^2 of 57.6mW/mm^2. To the authors' knowledge, these results demonstrate a record output power and P_{sat}/mm^2 for H-band amplifiers working around 270GHz.

RTu2F-4

A Linear and Efficient Power Amplifier Supporting Wideband 64-QAM for 5G Applications from 26 to 30GHz in SiGe:C BiCMOS

Tsung-Ching Tsai, Christian Bohn, Joachim Hebeler, Mehmet Kaynak, Ahmet Çağrı Ulusoy; KIT, Germany

Abstract: This paper presents a compact transformer-based linear and efficient power amplifier (PA) in 0.13-µm SiGe:C BiCMOS for 5G applications. To reduce the form factor, an ultra-compact neutralized cascode PA core is proposed, which achieves a state-of-the-art power density. To obtain a gain flatness at 5G NR band n257 (26.50–29.50GHz), transformer-based input and output matching networks are designed. The PA demonstrates a S_{21} 3-dB bandwidth (BW_{-3dB}) of 10.5GHz from 23.5 to 34GHz. At 28GHz/29GHz, the saturated output power (P_{sat}) are 22.7/22.4dBm with power-added efficiency (PAE) of 38.1/39.8%. The PA also supports 64- and 256-QAM modulated signal tests without digital pre-distortion (DPD). Over 26–30GHz, for 4.8Gb/s 64-QAM signals with peak-to-average power ratio (PAPR) 8.3dB at -25dB EVM, this PA continuously achieves >16dBm average power (P_{avg}) with >11% PAE.

Wednesday, 23 June 2021
10:00–11:40

Session RTu2G
Circuit Techniques for High-Speed Transceiver Front-Ends
Chair: Bahar Jalali Farahani, Acacia Communications, USA
Co-Chair: Alyssa Apsel, Cornell University, USA

RTu2G-1
A Sub-0.25pJ/Bit 47.6-to-58.8Gb/s Reference-Less FD-Less Single-Loop PAM-4 Bang-Bang CDR with a Deliberately-Current-Mismatch Frequency Acquisition Technique in 28nm CMOS

Xiaoteng Zhao, Yong Chen, Lin Wang, Pui-In Mak, Franco Maloberti, Rui P. Martins; University of Macau, China

Abstract: This paper reports a reference-less single-loop bang-bang clock and data recovery (BBCDR) circuit featuring fast and robust frequency acquisition without identifying the frequency error polarity. The key idea is a deliberately-current-mismatch charge-pump pair, which avoids the need of a complex high-speed data path or clock path during frequency acquisition. Prototyped in 28nm CMOS, our BBCDR covers a 47.6-to-58.8Gb/s PAM-4 input automatically. The achieved energy efficiency (≤0.25pJ/bit) and acquisition speed [9.8(Gb/s)/μs] compare favorably with the prior art.

RTu2G-2
A 128Gb/s PAM4 Linear TIA with 12.6pA/√Hz Noise Density in 22nm FinFET CMOS

Saeid Daneshgar, Hao Li, Taehwan Kim, Ganesh Balamurugan; Intel, USA

Abstract: This paper presents a 128Gb/s single-ended linear trans-impedance amplifier (TIA) intended for use in receivers for 400G Ethernet optical modules and co-packaged optics. The inverter-based shunt-feedback TIA is implemented in a 22nm FinFET CMOS process. It supports a record data rate of 128 Gb/s PAM4 and provides a DC trans-impedance gain of 59.3dB.Ω while dissipating only 11.2mW of power from a 0.8V supply. Series and shunt inductive peaking techniques are used to achieve a 3-dB trans-impedance bandwidth of 46GHz with a competitive input referred noise density of 12.6pA/√Hz. These results improve upon state-of-the-art BiCMOS/CMOS linear TIAs, demonstrating the potential for highly integrated, low-cost, high-sensitivity 100+G CMOS optical receivers in this process technology.

RTu2G-3

A 3GS/s >55dBFS SNDR Time-Interleaved RF Track and Hold Amplifier with >67dBc SFDR up to 3GHz in 22FDX

Enne Wittenhagen, Patrick Artz, Philipp Scholz, Friedel Gerfers; Technische Universität Berlin, Germany

Abstract: In this paper a high-linear 3 GS/s 2x TI RF TaH circuit driven by a single wideband bulk-controlled input buffer is presented. The measured output buffered TaH reveals an SFDR beyond 70 dBc up to 2.5 GHz and remains above 67 dBc till 3 GHz enabling subsampling. The SNDR is above 55 dBFS, with an input bandwidth of 4.5 GHz. The extracted clock jitter is about 45 fs rms and does not limit the SNDR up to 3 GHz. Interleaving mismatches, such as offset, gain, and time-skew between both lanes are calibrated digitally off-chip using a 37-tap FIR filter. Active body biasing is used to improve the TaH bandwidth, settling performance, leakage, and therewith the overall power consumption. The CMFB takes advantage of the body bias control by using the bulk as an input. The total power consumption of the TaH including the clock buffer is only 178mW from a triple 2 V/0.9 V/-0.8V supply.

RTu2G-4

A 6–31GHz Tunable Reflection-Mode N-Path Filter

Sandeep Hari, Cody J. Ellington, Brian A. Floyd; North Carolina State University, USA

Abstract: A 6–31 GHz reflection-mode N-path filter is implemented in 45 nm SOI technology. The filter is comprised of an on-chip hybrid coupler with through and coupled ports terminated with four-phase passive mixers. Each mixer provides a high impedance in-band and a 50-ohm impedance out-of-band, enabling reflection-mode bandpass filtering of the signal, with the center frequency set by the local-oscillator frequency. To increase selectivity, an active baseband load with adjustable bandwidth can be enabled to increase the roll-off to 12 dB/octave. The baseband loads between the two N-path mixers are shared to reduce size and power with the added benefit of creating a non-reciprocal filter response. Measurements show the filter can be tuned across 6–31 GHz with insertion loss <7 dB, typical return loss >10 dB, noise figure exceeding insertion loss by 1 dB at 6 GHz and 10 dB at 31 GHz, and in-band IIP3 of 1.4–6.3 dBm.

Wednesday, 23 June 2021
10:00–11:40

Session RTu2H
New Design Techniques for Frequency Generation
Chair: Wanghua Wu, Samsung, USA
Co-Chair: Andreia Cathelin, STMicroelectronics, France

RTu2H-1
An FBAR Driven -261dB FOM Fractional-N PLL
Dihang Yang, David Murphy, Hooman Darabi, Arya Behzad, Richard Ruby, Reed Parker; Broadcom, USA

Abstract: A 1mW -261dB FOM PLL with 91fs jitter is presented that combines a low-noise, high-frequency FBAR reference with the unity-gain harmonic-mixing (HM) PLL to minimize reference noise gain and avoid entirely the amplification of sigma-delta modulator quantization noise and fractional spurs, which, in turn, allows for a substantially larger loop bandwidth to suppress the VCO noise and speed settling.

RTu2H-2
A Sub-100fs $Jitter_{RMS}$, 20-GHz Fractional-N Analog PLL Using a BAW Resonator Based 2.5GHz On-Chip Reference in 22-nm FD-SOI Process
Sachin Kalia, Salvatore Finocchiaro, Ashwin Raghunathan, Bichoy Bahr, Tolga Dinc, Gerd Schuppener, Siraj Akhtar, Tobias Fritz, Baher Haroun, Swaminathan Sankaran; Texas Instruments, USA

Abstract: A 20-GHz Fractional-N Analog PLL leveraging a novel high-speed charge pump is presented. A fully integrable, on-chip 2.5GHz reference, using a MEMS-BAW resonator based DCO, allows a lower division-ratio and enhances suppression of charge pump (CP), phase-frequency detector (PFD) and, loop filter (LF) noise. Capability is built into the design to characterize the PLL with either BAW or external reference. Designed and fabricated in GlobalFoundries 22-nm FD-SOI process, the class-C transformer-coupled VCO is measured to be centered at ~19.7GHz with 16% tuning range while maintaining a flat |FOM| ~188dBc/Hz (10MHz offset) over the tuning range. The PLL measures an excellent jitter and $|FOM_J|$ of 65/92fs and ~249/245dB in integer/fractional modes, respectively.

RTu2H-3

Near-Field-Coupled Bondless BAW Oscillators in WCSP Package with 46fs Jitter

Bichoy Bahr, Ali Kiaei, Mahmud Chowdhury, Benjamin Cook, Swaminathan Sankaran, Baher Haroun; Texas Instruments, USA

Abstract: This paper presents a 2.5 GHz bulk acoustic wave (BAW) resonator-based oscillator in a wafer chip scale package (WCSP). Electro-Magnetic coupling is used to eliminate rigid galvanic connections between the BAW die and the CMOS oscillator die. The BAW die is attached to the latter with soft die attach, which eliminates stress coupling between the two, resulting in excellent aging performance for the oscillator. The CMOS oscillator circuit is significantly simplified owing to the inductor, which reduces power consumption, enhances oscillator stability, and lowers the phase noise. The presented oscillator achieves best-in-class 46 fs jitter in a sub-1mm^3 WCSP package with less than 15 ppm aging over 10 years.

RTu2H-4

Tuning-Less Injection-Locked Frequency Dividers with Wide Locking Range Utilizing 8th-Order Transformer-Based Resonator

Qiyao Jiang, Quan Pan; SUSTech, China

Abstract: This paper presents two tuning-less ultra-wide locking range (LR) injection-locked frequency dividers (ILFD). By utilizing an 8th-order transformer-based resonator, the LR can be improved significantly. Also, an inductive gain peaking technique is adopted to ensure start-up condition and achieve low power consumption. Two chips are fabricated in 40nm CMOS technology. The first chip exhibits a best-in-class LR of 104.5% from 28.8 to 91.9 GHz while consuming 5.8mW with a 0.9V power supply. The second chip achieves the best figure of merit (FoM) up to 26.6GHz/mW and 79.6% from 31 to 72 GHz LR with a 0.5V power supply.

Thursday, 24 June 2021
10:00–11:20

Session RTu3E
CMOS Transmitters and Amplifiers from RF to mm-Wave
Chair: Alexandre Giry, CEA-Leti, France
Co-Chair: Xun Luo, UESTC, China

RTu3E-1
A Sub-6GHz 5G New Radio Multi-Band Transmitter with a Switchable Transformer in 14nm FinFET CMOS

Wonjun Jung, Seunghoon Kang, Daechul Jeong, Ki Yong Son, Jongsu Lee, Jongwoo Lee, Ji-Seon Paek; Samsung, Korea

Abstract: This paper presents 2G/3G/4G/5G transmitter that has a compact die area and supports multi bands in 5G new radio (NR). The transmitter with inter-digitated switchable transformer is designed to support n77/n78/n79 of 5G FR1 bands (3.2GHz to 5GHz) and B46/B47 of V2X bands (5.125GHz to 5.925GHz). The transformer provides optimum transformed load impedance at the drive amplifier output with 3-stacked switches. The on-chip transformer with inter-digitated structure results in a high coupling factor to minimize the insertion loss. An inter-stage matching network between a mixer and a drive amplifier induces a channel flatness characteristic. The designed transmitter is fabricated using a 14nm FinFET CMOS process. It achieves a peak average output power of 7dBm and 2% under measured root mean square (rms) EVM in the case of DFT-s-OFDM 256QAM Full-RB signal, while satisfying the 3GPP specification. It also satisfies 1dB under channel flatness and the adjacent channel leakage ratio (ACLR) -43.2dBc in case of n77/n78, and -42.7dBc in case of n79, while consuming 295mW and 300mW dc power at 7.5dBm and 6.7dBm output power, respectively. The transmitter with inter-digitated switchable transformer has a size of 0.18mm^2.

RTu3E-2
A 0.7–8GHz High IF Frequency-Extended Transmitter Front-End with -47.1-dB EVM at 16QAM in 65-nm CMOS

Jiabing Liu[1], Shengjie Wang[1], Yue Gong[1], Dongdong Liu[2], Nie Hui[1], Chunyi Song[1], Qun Jane Gu[3], Zhiwei Xu[1]; [1]Zhejiang University, China, [2]Integrated Beam Tech, China, [3]University of California, Davis, USA

Abstract: This paper presents a 0.7–8 GHz transmitter front-end (TXFE) with high intermediate frequency (IF) input in 65 nm CMOS. To support high image rejection (IR) over a wide carrier frequency bandwidth, a local oscillator (LO), firstly used frequency-extended polyphase filter (PPF), is proposed. To obtain high linearity performance, a double balanced linearity enhanced multi-gate transistors (MGTR) up conversion mixer is utilized. To achieve an excellent IR over a broad signal bandwidth, a two-stage programmable PPF is employed to ensure a better than 0.2dB/2o quadrature

matching from 200 MHz to 550 MHz. The proposed TXFE fabricated in 65 nm CMOS may first achieve 168% relative bandwidth from 0.7–8 GHz for multi-band application. The TXFE achieves an EVM of -47.1 dB, when applying an 140 MHz 16 QAM signal at 2 GHz. It also obtains larger than 2 dBm output power and better than -20 dB image rejection with < 50 ns gain switching and < 200 ns frequency hopping time, which greatly relaxes the bandpass filter requirement before power amplifiers.

RTu3E-3

A 24.5–29.5GHz Broadband Parallel-to-Series Combined Compact Doherty Power Amplifier in 28-nm Bulk CMOS for 5G Applications

Seokhyeon Kim, Hyun-Chul Park, Daehyun Kang, Donggyu Minn, Sung-Gi Yang; Samsung, Korea

Abstract: This paper proposes a parallel-to-series combined Doherty power amplifier (PA) in 28-nm bulk CMOS technology that improves the operation bandwidth and minimizes the die area for the Doherty output network. The two-stage differential Doherty PA shows a saturated output power (P_{OUT}) of >18.8dBm and a peak power-added efficiency (PAE) of >30% at 27GHz CW. Under the 5G NR 64QAM OFDM signal (PAPR >10dB), the PA achieves a linear P_{OUT} of 12.4dBm and an average PAE of 20.2% at an EVM of -25dB. Over the frequency range of 24.5–29.5GHz, the PA exhibits a linear P_{OUT} of >11.2dBm and a PAE of >14.5% (DE >20.8%). This compact PA IC occupies 640×250μm^2 (core).

RTu3E-4

A 5G FR2 (n257/n258/n261) Transmitter Front-End with a Temperature-Invariant Integrated Power Detector for Closed-Loop EIRP Control

Chechun Kuo[1], Helen Zhang[1], Anirban Sarkar[1], Xiaohua Yu[1], Venumadhav Bhagavatula[1], Ashutosh Verma[1], Tienyu Chang[1], Ivan Siu-Chuang Lu[1], Daeyoung Yoon[2], Sangwon Son[1], Thomas Byunghak Cho[2]; [1]Samsung, USA, [2]Samsung, Korea

Abstract: This paper presents a multiband millimeter-wave transmitter front-end with an integrated power detector for enabling closed-loop power control. The power amplifier delivers an output power of 12.5dBm, PAE of 10% and EVM less than -25dB with CP-OFDM/64QAM/400MHz. A transformer-based PA output matching-network is proposed that presents the PA with an optimal load over the 5G frequency bands from 24.5–29.5GHz, while suppressing the second harmonic power to meet the stringent 5G emission regulation. A novel integrated power-detector (PDET) which employs a current-mode SAR ADC to improve temperature robustness of power tracking with antenna VSWR variations.

Thursday, 24 June 2021
10:00–11:20

Session RTu3F
RF and mm-Wave VCOs
Chair: Ehsan Afshari, University of Michigan, USA
Co-Chair: Pietro Andreani, Lund University, Sweden

RTu3F-1
A 10.7–14.1GHz Reconfigurable Octacore DCO with -126dBc/Hz Phase Noise at 1MHz Offset in 28nm CMOS

Lorenzo Tomasin[1], Giovanni Boi[2], Fabio Padovan[2], Andrea Bevilacqua[1]; [1]Università di Padova, Italy, [2]Infineon Technologies, Austria

Abstract: This paper presents an octacore DCO, implemented in a 28 nm CMOS technology, able to achieve an outstanding phase noise performance: -126 dBc/Hz at 1MHz offset from the 10.7GHz carrier with 173mW power consumption. The design is scalable, as the network coupling the oscillator cores can be reconfigured allowing to switch off some cores to save power without incurring in any additional phase noise penalty other than the one expected from the reduction of the number of the active cores. The DCO achieves a 27% tuning range with 6MHz frequency resolution.

RTu3F-2
A 2.3-to-3.2GHz Class-G Impedance-Modulation Power Oscillator with 10dBm Peak P_{out} and 39%/37%/33%/30% Efficiency at 0/3/6/9dB PBOs

Yiyang Shu[1], Huizhen Jenny Qian[1], Xiang Gao[2], Xun Luo[1]; [1]UESTC, China, [2]Zhejiang University, China

Abstract: In this paper, a Class-G impedance-modulation power oscillator is proposed to enhance the efficiencies at multiple PBOs. With the switch-combined reconfigurable matching-resonator, the output matching is optimized along with the tuning of oscillation frequency. Meanwhile, the digitally controlled tail resistor array is used to continuous tune the output power. The proposed power oscillator is fabricated in a 40-nm CMOS technology. Measurements exhibit a 33% tuning range from 2.3 to 3.2GHz. The peak output power is 10dBm while the efficiencies at 0/3/6/9dB PBOs are 39%, 37%, 33%, and 30%, respectively. The 1MHz-offset phase noise is -131.5 to -127.2dBc/Hz over the operation frequency.

RTu3F-3

A Novel Miniaturized Tri-Band VCO Utilizing a Three-Mode Reconfigurable Inductor

Seongwoog Oh, Jungsuek Oh; Seoul National University, Korea

Abstract: A novel miniaturized tri-band complementary metal-oxide-semiconductor (CMOS) voltage-controlled oscillator (VCO) utilizing a three-mode reconfigurable inductor is proposed. The reconfigurable inductor consists of primary and secondary windings with a center loop connected to each winding center-tap to enable three-mode operation. By adjusting the diameter of each winding and loop, the equivalent inductance for each mode can be designed independently, resulting in a high degree of freedom for a tri-band VCO with minimal Q-factor degradation. The VCO implemented in a 28nm CMOS process shows frequency tuning ranges of 16.78–20.13GHz, 19.8–24.15GHz, and 33–41.13GHz for each mode with corresponding phase noise and tuning range figure-of-merit (FoM_T) values of -190.1, -190.9, -194.6dBc/Hz. The fabricated chip consumes 12.72mW and occupies a core area of 0.043mm^2.

RTu3F-4

A 3.1–51GHz, Sub-8mW, Single-Core LC VCO Based on a Novel Compact Tunable Transmission Line (CTTL) Resonator in 28nm FDSOI CMOS

Thomas Tapen[1], Andreia Cathelin[2], Alyssa Apsel[1]; [1]Cornell University, USA, [2]STMicroelectronics, France

Abstract: The adoption of 5G standards requires new wireless devices to support not only traditional RF bands, but also mmW frequencies up to and beyond 40GHz. Such mmW hardware typically requires narrowband LC resonant circuits for efficient, low-noise operation. For widely-tuned software-defined systems, multi-octave LC tuning is not achievable due to the lack of a practical, solid-state tunable inductive element, limiting the mmW performance of software-defined radios. In this paper, we present a novel, compact, lumped/distributed LC-equivalent resonator capable of continuous tuning over more than four octaves in frequency while maintaining a practical quality factor in an unmodified 28nm FDSOI CMOS for the first time. This resonator is used to implement a cross-coupled LC VCO tunable from 3.1 to beyond 51GHz requiring less than 0.208mm^2 of area, less than 8mW of power, and achieving a state of the art peak FOM_T for multi-octave tunable mmW VCOs of -198.2dBc/Hz.

Thursday, 24 June 2021
10:00–11:20

Session RTu3G
RF Systems for Emerging Wireless Applications
Chair: Vadim Issakov, TU Braunschweig, Germany
Co-Chair: Mona M. Hella, Rensselaer Polytechnic Institute, USA

RTu3G-1
A Fully-Digital 0.1-to-27Mb/s ULV 450MHz Transmitter with Sub-100μW Power Consumption for Body-Coupled Communication in 28nm FD-SOI CMOS

Guillaume Tochou[1], Robin Benarrouch[1], David Gaidioz[1], Andreia Cathelin[1], Antoine Frappé[2], Andreas Kaiser[2], Jan Rabaey[3]; [1]STMicroelectronics, France, [2]IEMN (UMR 8520), France, [3]University of California, Berkeley, USA

Abstract: A 0.5 V fully-digital 450 MHz transmitter for surface wave capacitive body-coupled communications is realized in 28 nm FD-SOI CMOS and consumes 17 to 76 μW for data rates from 0.1 to 27 Mb/s with up to 14%system efficiency. The heavily duty-cycled transmitter uses a 90 MHz free-running oscillator and edge combiners to generate OOK Gaussian-shaped pulses through a switched-capacitor PA. Body-biasing allows frequency tuning and adaptive efficiency optimization as a function of data rate.

RTu3G-2
A mm-Wave Transmitter MIMO with Constellation Decomposition Array (CDA) for Keyless Physically Secured High-Throughput Links

Naga Sasikanth Mannem, Tzu-Yuan Huang, Elham Erfani, Sensen Li, Hua Wang; Georgia Tech, USA

Abstract: Conventional phased array beamforming realizes spatial physical security but is effective only for large arrays, while most cryptographic algorithms require security key exchanges and pose large computation overhead and latency to handle Gbit/s throughput. We propose a Constellation-Decomposition Array (CDA) MIMO technique to achieve a highly secured yet keyless wireless link for low-element count arrays. The CDA MIMO spatially combines lower order QAMS, so that the high-order QAM is observed only in the target direction and shows large distortions in other directions. Temporal swapping of the decomposed CDA constellations among MIMO elements further enhances the security. The proposed scheme is demonstrated on an 8-element 25–34GHz TX MIMO array in 45nm CMOS SOI with on-pcb antennas. Over-the-air 4-element MIMO measurements achieve an information beamwidth of 5°/10° at up-to 3Gbit/s by forming a 64QAM signal using three QPSKs or 16QAM/QPSK, respectively, demonstrating a mm-Wave wireless link with simultaneous security and high throughput.

RTu3G-3

A 0.31THz CMOS Uniform Circular Antenna Array Enabling Generation/ Detection of Waves with Orbital-Angular Momentum

Muhammad Ibrahim Wasiq Khan[1], Jongchan Woo[1], Xiang Yi[1], Mohamed I. Ibrahim[1], Rabia Tugce Yazicigil[2], Anantha Chandrakasan[1], Ruonan Han[1]; [1]MIT, USA, [2]Boston University, USA

Abstract: This paper reports the first chip-based demonstration (at any frequency) of a CMOS front-end that generates and receives electromagnetic waves with rotating wave phase front (namely orbital angular momentum or OAM). The chip, based on a uniform circularly placed patch antenna array at 0.31THz, transmits reconfigurable OAM modes, which are digitally switched among the m=0 (plane wave), +1 (left-handed), -1 (right-handed) and superposition (+1)+(-1) states. The chip is also reconfigurable into a receiver mode that identifies different OAM modes with >10dB rejection of unintended modes. The array, driven by only one active path, has a measured EIRP of -4.8dBm and consumes 154mW of DC power in the OAM source mode. In the receiver mode, it has a measured conversion loss of 30dB and consumes 166mW of DC power. The output OAM beam profiles and mode orthogonality are experimentally verified and a full silicon OAM link is demonstrated.

RTu3G-4

An 84.48Gb/s CMOS D-Band Multi-Channel TX System-in-Package

Abedelaziz Hamani, Francesco Foglia-Manzillo, Alexandre Siligaris, Nicolas Cassiau, Benjamin Blampey, Frederic Hameau, Cedric Dehos, Antonio Clemente, Jose Luis Gonzalez-Jimenez; CEA-Leti, France

Abstract: This paper presents an in-package D-band wireless module co-integrating an innovative channel bonding transmitter IC in 45 nm CMOS PDSOI technology and a patch antenna fabricated using a low-cost printed circuit board process. The transmitter is composed of two up-conversion chains with dedicated millimeter-wave local oscillator generators and operates over contiguous sub-bands around 147.96 GHz. The two sub-band signals are combined off-chip using a substrate integrated waveguide diplexer and radiated by a four-patch antenna array realized on the same laminate substrate. The total output band spans from 139.3 to 156.6 GHz. A data rate of 84.48 Gb/s is demonstrated using 64-QAM. The radiated power is 3.8 dBm at the output 1 dB compression point. The chip consumes 600 mW from a 1-V voltage supply and occupies a compact area of 4.8mm^2.

Thursday, 24 June 2021
10:00–11:20

Session RTu4E
mm-Wave Circuits for Emerging Applications
Chair: Jeyanandh Paramesh, Carnegie Mellon University, USA
Co-Chair: Hongtao Xu, Fudan University, China

RTu4E-1
A 4Rx, 4Tx Ka-Band Transceiver in 40nm Bulk CMOS Technology for Satellite Terminal Applications

Alan Chi-Wai Wong[1], Gabriele Devita[1], Shi-Ming Wu[1], Franco Lauria[1], Majd Eid[1], Omotade Illuromi[1], Samson Ogunkunle[1], Alessandro Modigliana[2]; [1]EnSilica, UK, [2]Satellite Applications Catapult, UK

Abstract: This paper presents a K/Ka-band transceiver for phased array satellite mobile ground terminal applications. The transceiver integrates four receiver (Rx) RF paths operating at 17~21GHz and the four transmitter (Tx) RF paths operating at 27~30GHz, each with independent 0.5dB gain and 5-bit phase control to support analog RF beamforming. Each Rx RF path is summed in an integrated passive combiner before an IQ frequency down conversion stage driven with a LO frequency doubler. Each Tx RF path is driven from an integrated IQ modulator clocked with an LO frequency tripler with an active power splitter. The Rx and Tx baseband (BB)/IF paths consist of 325MHz wide IQ VGAs and filtering to support up to 650MHz instantaneous bandwidth. The transceiver achieves 3.3dB NF and +10dBm output power per RF path in Rx and Tx modes respectively, whilst consuming 200mW in 4RF+BB Rx mode and 500mW in BB+4RF Tx mode. It is fabricated in 40nm bulk CMOS and occupies 10.7mm^2.

RTu4E-2
A 20–40GHz High Dynamic Range HBT N-Path Receiver with 8.9dBm OOB B1dB and 8.55dB NF Consuming 130mW

Robin Ying, Alyosha Molnar; Cornell University, USA

Abstract: A millimeter(mm)-wave widely-tunable mixer-first noise-cancelling receiver is demonstrated in 130 nm BiCMOS where an HBT LNTA loaded by a quadrature mixer is protected by an HBT-based N-path filter with linear-periodically-time-varying feedback for impedance transparency providing bandpass filtering. 20–40 GHz tunable, dual-resonant LO buffers use inductance to resonate out the mixer capacitance but still generate 25% duty-cycle LO pulses to reduce overlap-induced loss. The receiver simultaneously achieves +8.9 dBm OOB B1dB and 8.55 dB NF while functioning across an octave in the mm-wave band.

RTu4E-3

A 2-Channel 136–156GHz Dual Down-Conversion I/Q Receiver with 30dB Gain and 9.5dB NF Using CMOS 22nm FDSOI

Changtian Wang, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a D-band 2-channel dual down-conversion receiver front-end with a sliding IF architecture in 22nm FDSOI process. A fully-differential D-band low-noise amplifier (LNA) followed by an active double-balanced mixer is first used and down-converts the 137–157 GHz RF signal to an intermediate frequency (IF) of 31–40 GHz. The IF signal is split into I and Q channels and is down-converted to zero-IF output I/Q signals using a passive mixer for low 1/f noise. A ×6 LO (17.5 GHz to 35 GHz and to 105 GHz) chain is included on the chip and provides the required LO for both mixers. The receiver achieves a measured peak gain of 27–30 dB, a noise figure of 9–10.5 dB at 136–154 GHz, a simulated output flicker noise corner frequency of 25 kHz and consumes 395 mW for both channels and the LO chain. The measured input P1dB is -29 dBm resulting in a high SNR for wide bandwidth signals. A measured EVM of 4.3–4.8% was achieved at 1–2 Gbaud for 16-QAM and 64-QAM waveforms. To the authors' knowledge, this work presents the first D-band CMOS I/Q receiver with application areas in dual-polarized receivers for point-to-point systems and digital beamforming MIMO arrays.

RTu4E-4

A 290GHz Low Noise Amplifier Operating Above $f_{max}/2$ in 130nm SiGe Technology for Sub-THz/THz Receivers

Sumit Pratap Singh, Timo Rahkonen, Marko E. Leinonen, Aarno Pärssinen; University of Oulu, Finland

Abstract: This paper presents the design of a low noise amplifier (LNA) operating at center frequency 290 GHz in 130 nm SiGe BiCMOS technology with f_t/f_{max} of 300 GHz/450 GHz. The LNA consists of four stages of pseudo-differential cascode topology. Each stage is tuned and matched at different resonant frequency to obtain broadband frequency response around center frequency. This LNA provides 12.9 dB of gain at center frequency 290 GHz and 11.2 dB at 300 GHz. The 3-dB bandwidth is measured to be 23 GHz and simulated noise figure is 16 dB. The LNA draws 68 mA current from 2V supply. It shows the potential of silicon technologies to operate as high as $2/3(f_{max})$ with decent gain and linearity at 300 GHz range. To the authors' knowledge, this LNA achieves, without any gain-boosting technique, the highest gain at $2/3(f_{max})$ in SiGe technology.

Thursday, 24 June 2021
10:00–11:40

Session RTu4G
Efficient Radios for IoT, GPS, WiFi, and Cellular
Chair: Roxann Broughton-Blanchard, Analog Devices, USA
Co-Chair: Arun Paidimarri, IBM T.J. Watson Research Center, USA

RTu4G-1
An Electrical Balance Duplexer for FDD Radios That Isolates TX from RX Independently in Two Bands

Kejian Shi[1], Hooman Darabi[2], Asad A. Abidi[1]; [1]University of California, Los Angeles, USA, [2]Broadcom, USA

Abstract: An Electrical Balance Duplexer (EBD) supports dual-band TX-RX isolation enabling FDD operation at 5–7 GHz for Wi-Fi 6/6E. A programmable network in the EBD can balance the antenna impedance (Z_{ANT}) in the TX channel and RX channel independently. The EBD provides > 40 dB isolation in an 80MHz channel bandwidth in the TX band (5–6 GHz), for any $Z_{ANT}(f_{TX})$ within VSWR= 2, and independently in the RX band (6–7 GHz) when $Q_{ANT} < 4.3$. The EBD is designed for < 4 dB RX IL and < 3.8 dB TX IL, and it supports +29dBm TX output.

RTu4G-2
An LTE-A Multimode RF Transmitter with -64.5dB B41 CIM3 Suppression and 256QAM/HPUE Capability in 28nm CMOS

Carl Bryant[1], Manel Collados[1], Ben Abdeljelil[1], Paul Fowers[1], Mohammed Hassan[1], David Ivory-Cave[1], Dimitris Nalbantis[1], Jon Strange[1], Levine Chen[2], Johoo Lin[2]; [1]MediaTek, UK, [2]MediaTek, Taiwan

Abstract: Multimode cellular transceivers need to simultaneously meet the high linearity and emissions requirements of LTE-A, the accurate power control of 3G, and the stringent noise of 2G. This paper presents an LTE-A multimode transmitter capable of fulfilling the stringent output power and emissions requirements of the band 41 high power user equipment (HPUE) standard. The presented current-mode architecture provides good linearity and high suppression of counter-intermodulation (CIM) products, achieving -64.5dBc CIM3 in band 41 while transmitting 6dBm.

RTu4G-3

A 2.1mW -109dBm NB-IoT Wake-Up Receiver

Trevor J. Odelberg, Jaeho Im, David D. Wentzloff; University of Michigan, USA

Abstract: A low-power standard-compliant NB-IoT wake-up receiver (WRX) is presented. The WRX is designed as a companion radio to a full NB-IoT receiver, only operating during discontinuous RX modes (DRX and eDRX), which allows the full high-power radio to turn off while the wake-up receiver efficiently receives NB-IoT Wake-Up Signals (WUS). The fabricated receiver achieves 2.1mW power at -109dBm sensitivity with 180kHz bandwidth over the 750–960MHz bands. The WRX is fabricated in 28nm CMOS and consumes 5x less power than the best previously published traditional NB-IoT receivers. This work is the first designed dedicated wake-up receiver for the NB-IoT protocol and demonstrates the benefits of utilizing a WRX to reduce power consumption of NB-IoT radios.

RTu4G-4

A 300μW Bluetooth-Low-Energy Backchannel Receiver Employing a Discrete-Time Differentiator-Based Coherent GFSK Demodulation

Omar Abdelatty[1], Abdullah Alghaihab[1], Yaswanth K. Cherivirala[1], Sumanth Kamineni[2], Benton Calhoun[2], David D. Wentzloff[1]; [1]University of Michigan, USA, [2]University of Virginia, USA

Abstract: This paper presents a 300μW backchannel receiver (RX) compatible with the Bluetooth-Low-Energy (BLE) standard for ultra-low power Internet-of-Things (IoT) applications. A PLL-less, mixer-first zero-IF architecture is proposed to achieve the low power operation featuring an antenna-chip co-design for lossless quadrature (I/Q) generation in the RF path. A novel 10μW switched-capacitor differentiator-based GFSK demodulator is presented. The demodulator exhibits a robust operation under I/Q phase and amplitude imbalances and operates at a 1MHz baseband clock frequency. The proposed backchannel communication within the packet's payload is achieved through 2× data repetition. The chip is designed and fabricated in CMOS 40nm technology. The RX achieves -69dBm sensitivity for 0.1% BER at 0.5Mbps effective data rate.

RTu4G-5

A Compact, Reconfigurable Receiver for IRNSS/GPS/Galileo/Beidou

Vijaya Kumar Kanchetla, Ajinkya Kharalkar, Jeffin Joy, Swetha Clara Jose, Santosh Kumar Khyalia, Shubham Jain, Mukul Pancholi, Syed Hameed, Amitesh Kumar Tripathi, Sumit Khalapure, Rajesh Zele; IIT Bombay, India

Abstract: This paper presents a compact fully integrated low-IF reconfigurable receiver for satellite navigation systems that use L1, L2, L5, and S frequency bands with 2–4 MHz signal bandwidth. A new wideband input matched balun Low-Noise amplifier (LNA) with noise cancellation is used to avoid external matching. A new DC offset correction circuit is designed in the Variable Gain Amplifier (VGA) to avoid signal saturation. A single fully integrated on-chip Fractional-N Phase-Locked Loop (PLL) is designed to generate the local oscillator (LO) for all the frequency bands. The receiver is fabricated in 65 nm CMOS technology, and it provides a maximum gain of 101 dB with gain dynamic range of 51 dB. It achieves a minimum noise figure of 3.8 dB and an image rejection ratio (IMRR) of 28 dB. It draws a current of 34.2–42 mA from a 1.2 V supply while occupying an active die area of 1.96 mm^2. The die is packaged in a 32-pin QFN package.

RFIC WORKSHOPS

Friday 25 JUNE 2021

Workshops are offered via the virtual platform on Friday 25 June 2021. Three full day workshops (WSB, WSE and WSK) will run from 10:00 to 16:00, while the remaining workshops are half day workshops from 10:00 to 14:00 (WSA, WSC, WSD, WSF, WSG, WSH, WSI, WSJ, WSL).

Workshop WSA (half day, 10:00–14:00)
Low Power Radios and Wireless Technologies for Indoor Positioning and Localization

Sponsor: **RFIC**

Organizers: **Arun Paidimarri**, *IBM T.J. Watson Research Center*
Yao-Hong Liu, *imec*
Oren Eliezer, *Ambiq*
Gernot Hueber, *Silicon Austria Labs*

Abstract: The Internet of things and low-power wireless devices encompass many protocols and standards, each optimized for their specific set of applications, with the unifying themes being battery-operation, low average data rates, power-efficient processing, low cost-size and extensive integration with sensors, processors and power management. This workshop presents several talks on the architectures and circuits for existing standards and applications, and explores research that will inform the next generation of these technologies. Application spaces that are increasingly gaining traction are wearables and indoor localization and positioning, with prime examples being smart buildings, distance-bounded security, and, most recently, COVID tracking. This workshop will also cover several state-of-the-art technologies in wearable devices and in indoor localization in the context of low-power wireless communications.

Speakers:

1. "Ultra-Wideband and Indoor Localisation Systems", **Dries Neirynck**, *Qorvo*
2. "Sub-Microwatt Receivers for Near Zero-Power and Energy Harvesting Wireless Sensor Nodes", **Steven M. Bowers**, *University of Virginia*
3. "Radio Architectures and Circuits for Low-Power Wide Area Networks", **Danielle Griffith**, *Texas Instruments*
4. "Low-Power Radio Design Challenges and Solutions for Wearables", **Mohammad Hekmat**, *Mojo Vision*
5. "FSK Technology for Indoor Vital Signs Sensing and Human Tracking", **Changzhi Li**, *Texas Tech University*
6. "Enabling Standards-Compliant Wireless Communications at >100x Lower Power", **Patrick Mercier**, *University of California, San Diego*
7. "An Ultra-Low-Power (ULP) Phase-Tracking Receiver for IoT Applications", **Teerachot Siriburanon**, *University College Dublin*
8. "Accurate Distance Measurement Using Narrowband Bluetooth Devices", **Jac Romme**, *imec*

Workshop WSB (full day, 10:00–16:00)
100–300GHz mm-Wave Wireless for 0.1–1Tb/s Networks

Sponsor: **RFIC**

Organizers: **Jane Gu**, *University of California, Davis*
Mark Rodwell, *University of California, Santa Barbara*

Abstract: Wireless systems using higher (100–300GHz) mm-wave carrier frequencies will benefit from large available bandwidths and, given the very short wavelengths, massive spectral re-use via massive spatial multiplexing. Simple radio link budget analysis suggests that ~1Tb/s capacities are feasible in both point-multipoint network hub and point-point backhaul links. But, range is limited by high Friss path loss and high foul-weather attenuation, and beams are readily blocked. We will examine the design, the technical challenges, and the potential design of such systems, including link architecture, link budgets, radio propagation characteristics, array tile module and antenna design, MIMO channel estimation, massive MIMO beamformer dynamic range analysis, digital beamformer design, design of mesh networks to accommodate beam blockage, RF front-end design in CMOS, SiGe and III-V technologies, and estimates of system DC power consumption as a function of architecture.

Speakers:

1. "Tbps Massive MIMO: Mapping System Performance to Hardware Specs", **Sundeep Rangan[1], Upamanyu Madhow[2]**, *[1]NYU, [2]University of California, Santa Barbara*
2. "Outdoor Propagation Characteristics at 100–300GHz", **Andreas Molisch**, *University of Southern California*
3. "High-Efficiency and High-Power Amplifiers for Transmitters Above 100GHz", **James F. Buckwalter**, *University of California, Santa Barbara*
4. "Energy Efficiency Analysis of MIMO Systems at 100–300GHz", **Danijela Cabric**, *University of California, Los Angeles*
5. "Energy and Spectrally Efficient Communication Using mm-Wave and sub-THz Bands", **Ali M. Niknejad**, *University of California, Berkeley*
6. "A Multiplierless Beamspace Transform Engine for Wideband mm-Wave–THz Communication Systems", **Christoph Studer**, *Cornell University*
7. "140GHz CMOS SOI Beamforming ICs for Phased-Array Applications", **Gabriel M. Rebeiz**, *University of California, San Diego*
8. "100–300GHz Systems Architectures and Applications", **Mark Rodwell**, *University of California, Santa Barbara*

Workshop WSC (half day, 10:00–14:00)
CMOS mm-Wave Imaging Radars: State-of-the-Art and a Peek into the Future!

Sponsor: **RFIC**

Organizers: **Vadim Issakov**, *TU Braunschweig*
Venkatesh Srinivasan, *Texas Instruments*

Abstract: Advances in mm-wave CMOS technology has resulted in fully integrated mm-wave radar sensors that offer a cost-effective and robust solution to automotive safety, provide accurate industrial sensing and enable gesture recognition. This workshop will feature technical experts from both academia and industry to present the state-of-the-art in mm-wave CMOS technology such as all-digital architectures, higher carrier frequencies, sophisticated signal processing and machine learning. These technologies promise to improve the achievable accuracy and push performance levels further. Speakers will also share their view of the next steps in this space and the possibilities for the future.

Speakers:

1. "Signal Processing for Imaging Radar System", **Dan Wang**, *Texas Instruments*
2. "mm-Wave Radar for Short and Ultra-Short Distance", **Hao Gao**, *Technische Universiteit Eindhoven*
3. "mm-Wave Radar for Gesture Detection: Circuit Design and System Considerations", **Matteo Bassi, Johannes Rimmelspacher**, *Infineon Technologies*
4. "From Detection to Classification: the Next Generation of Automotive Radars", **Juergen Hasch**, *Robert Bosch*
5. "Continuous-Time Delta-Sigma Modulator (CT-DSM) Based PLL for Radar", **Michael P. Flynn**, *University of Michigan*
6. "CMOS THz Comb Radar: On-Chip Parallelism for Broadband Electromagnetic Spectral Sensing", **Ruonan Han**, *MIT*
7. "A Single-Chip Digital Approach to MIMO Radars", **Marius Goldenberg**, *Uhnder*
8. "A 145GHz FMCW Radar Based in 28nm CMOS", **Akshay Visweswaran**, *imec*

Workshop WSD (half day, 10:00–14:00)
Coherent Optical Communications for Cloud Data Centers, Metro, and Submarine Networks

Sponsor: **RFIC**

Organizers: **Ricardo Aroca**, *Acacia Communications*
Bahar Jalali Farahani, *Acacia Communications*

Abstract: The introduction of IoT (Internet of things) and cloud computing has accelerated the demand for higher bandwidth and higher capacity networks. Coherent detection, where the phase information of the optical carrier provides higher signal-to-noise ratios, has gained an ever-increasing momentum. Today coherent communication dominates long-haul networks operating with data rates beyond 400 Gbps per wavelength. Thanks to advancements in digital signal processing that leverage ultra-low power implementations in deep submicron technologies (i.e. 7nm), the cost and power of coherent transponders are becoming competitive for short reach networks as well (inter and intra-data centers). Reducing the cost and enhancing the overall performance of such networks are only achievable through highly integrated solutions that encompass complex digital signal processing algorithms, state-of-the-art transimpedance amplifiers and modulator drivers, and integrated silicon photonics. The co-design and co-optimization become the key factor in further power and performance scaling of coherent transponders. Different elements of optical communication systems have been subject of prior workshops at RFIC. This workshop, however, brings together a multidisciplinary team of expertise to inform audience of technology advancements in all key components that make up an integrated optical communication system. Co-design, co-optimization, and hybrid integration will be the theme and focus of this workshop and are addressed by several speakers from different perspectives. Emerging applications for coherent detection such as LiDAR will be discussed and utilizing emerging technologies of AI and machine learning in next generation of optical communication systems will be explored.

Speakers:

1. "Signal Processing Techniques That Impact Optical Communications", **Alan E. Willner**, *University of Southern California*
2. "Recent Advancements in Integrated Photonics", **Chris Doerr**, *Acacia Communications*
3. "Market Forces and Network Evolution", **Joel Goergen**, *Cisco Systems*
4. "Energy-Efficient Coherent Optical Transceivers Using Silicon Photonic and Si CMOS-SiGe BiCMOS RFICs", **James F. Buckwalter**, *University of California, Santa Barbara*
5. "Coherent LiDAR with Optical Phased Arrays", **Christopher Poulton**, *Analog Photonics*
6. "Applications of Photonics in AI and Machine Learning", **Young-Kai Chen**, *DARPA*
7. "ADCs and DACs for Coherent Transmission Beyond 400G", **Ian Dedic**, *Acacia Communications*

Workshop WSE (full day, 10:00–16:00)
Cryogenic Electronics for Quantum Computing and Beyond: Applications, Devices, and Circuits

Sponsor: **RFIC**

Organizers: **Joseph Bardin**, *UMass Amherst*
Fabio Sebastiano, *Technische Universiteit Delft*

Abstract: With rapid advances in the performance of qubit technology, quantum computing has attracted intense interest of the media and research community. Several opportunities have emerged for circuit designers, as the quantum devices require classical electronics for their control and read-out. In particular, cryogenic operation of the electronics is required to allow their proximity to quantum processors, which are typically cooled to cryogenic temperature in the range of 20 mK. However, applications of cryogenic electronics reach beyond quantum computing. These applications include both the realization of interfaces for devices such as quantum processors, which must be operated cryogenically, as well as the implementation of systems that outperform their room temperature counterparts (e.g., front-ends for radio telescopes). This workshop will present an overview of cryogenic electronics from applications down to device operation, with a specific emphasis on integrated circuits. The workshop consists of 8 talks from experts in the field, organized into three main themes: cryogenic applications, cryogenic devices, and cryogenic circuits. First, typical applications requiring operation at cryogenic temperatures will be presented to highlight requirements for electronic components, their current limitations, and future perspectives. The first talk will focus on quantum-computing applications, while the second targets the need of cryogenic detectors for particle physics. Next, the operation of semiconductor devices at cryogenic temperatures will be discussed, including industry-standard semiconductors, such as SiGe (third talk) and CMOS (fourth talk), to point out advantages and drawbacks in device operation, always with an eye to their use into practical circuits. Finally, four design examples of integrated circuits employing SiGe, bulk CMOS and FD-SOI CMOS and targeting low-noise amplification or quantum computing will be shown, thus practically demonstrating circuit-design techniques and architecture to exploit (or circumvent) cryogenic design operation to meet the system requirements.

Speakers:

1. "A Cryo-CMOS Control Interface for a Semiconductor-Based Quantum Computer", **Alireza Moini[1], Yuanyuan Yang[2], David Reilly[3], Michael Manfra[4], Kushal Das[1], Sebastian Pauka[3], Geoff Gardner[1], Rachpon Kalra[1]**, *[1]Microsoft, [2]Morse Micro, [3]University of Sydney, [4]Purdue University*
2. "Cryogenic Detectors and Electronics for Particle Physics", **Gianluigi Pessina**, *INFN*
3. "The Opportunities and Challenges of Using SiGe HBTs in the Deep Cryogenic Temperature Environment", **John D. Cressler**, *Georgia Tech*
4. "MOSFET Compact Modeling down to Cryogenic Temperatures", **Arnout Beckers, Christian Enz, Farzan Jazaeri**, *EPFL*
5. "Low-Power Silicon Germanium Cryogenic Low Noise Amplifiers", **Shirin Montazeri**, *Google*

6. "Cryogenic CMOS Architectures for Large-Scale Quantum Computers", **Fabio Sebastiano[1], Masoud Babaie[1], Edoardo Charbon[2], Stefano Pellerano[3]**, *[1]Technische Universiteit Delft, [2]EPFL, [3]Intel*
7. "Testing Requirements for Emerging Single-Chip Cryogenic Mixed-Signal Quantum Processors in Production FDSOI CMOS Technology", **Mecca Gong, Utku Alakusu, Sadegh Dadash, Sorin P. Voinigescu, Lucy Wu, Shai Bonen**, *University of Toronto*
8. "Quantum Computer on a Chip", **Hongying Wang[1], Mike Asker[2], Panagiotis Giounanlis[1], R. Bogdan Staszewski[1], Elena Blokhina[1], Alireza Esmailiyan[2], Andrii Sokolov[1], Teerachot Siriburanon[1], Imran Bashir[2], Dirk Leipold[2]**, *[1]University College Dublin, [2]equal1*

Workshop WSF (half day, 10:00–14:00)
Fully Integrated Silicon vs. Hybrid RFFE Systems for mm-Wave 5G Highly Efficient PA Design Trade-Offs

Sponsor: **RFIC**

Organizers: **Debopriyo Chowdhury**, *Broadcom*
Donald Y.C. Lie, *Texas Tech University*
Patrick Reynaert, *KU Leuven*

Abstract: Low noise amplifiers (LNA), power amplifiers (PA), switches and phase shifters can all be integrated into one silicon RF-front-end (RFFE) IC for mm-wave 5G, and even multichannel integration may be possible. However, the advantages in costs, robustness, and manufacturability for an all-silicon RFFE IC approach is not yet clear, when compared to a hybrid III-V-silicon solution for 5G. The power efficiency of mm-wave 5G broadband PA is considerably lower than their 4G counterparts, and GaN-GaAs III-V based PAs have high output power and good efficiency vs. those of silicon-based PAs. At the same time, hybrid integration approaches increase rapidly in cost as complexity increases, as will be covered in this workshop. Can newer technologies enable an all-silicon RF front end that can match the performance of hybrid solutions? As we go to mm-wave frequencies, achieving high efficiency and linearity simultaneously for the PA becomes extremely challenging, and novel RF linearization techniques are required to improve these 5G mm-wave PAs. All-silicon solutions with superstrates for antennas are currently being investigated, and we will discuss the PA-Antenna and PA-Package co-design for 5G MIMO PAs as well.

Speakers:
1. "The Final Showdown : GaN-Si and CMOS for 5G and 6G mm-Wave Applications", **Marc Rocchi**, *OMMIC*
2. "mm-Wave PA Design in Bulk and FinFET CMOS", **Patrick Reynaert**, *KU Leuven*
3. "III-V Semiconductors for 5G mm-Wave FEM and High Efficiency PA Design", **Eli Reese**, *Qorvo*
4. "IC and Package Co-Design Techniques & Technologies for High Efficiency Linear PA Modules", **Pascal Reynier**, *CEA-Leti*

5. "Co-Integration of CMOS and III-V for mm-Wave 5G", **Aritra Banerjee**, *imec*
6. "CMOS RF for mm-Wave Frontends", **H.-H. Hsieh**, *TSMC*
7. "Benefits of RFSOI Technology for mm-Wave PA & Front End Applications", **Baljit Chandhoke**, *GLOBALFOUNDRIES*

Workshop WSG (half day, 10:00–14:00)
Highly Linear and Linearized Power Amplifiers for mm-Wave Communications

Sponsor: **RFIC**

Organizers: **Margaret Szymanowski**, *Crane Aerospace & Electronics*
Jeffrey S. Walling, *Skyworks Solutions*

Abstract: Presently, power amplifiers do not fulfill all of the requirements of linearity, energy efficiency, and bandwidth that are required for mm-wave operation for 5G and future communications, particularly for the user equipment. New techniques are required in the design of ultra-high linearity power amplifiers, or through improved linearization, efficiency enhancement and bandwidth extension techniques to dramatically improve the performance to open the full potential of future communications systems. It is noted that all aspects of mm-wave PA design become more challenging when placed into arrays with non-negligible element-to-element coupling. This workshop will explore power amplifier designs in the mm-wave spectrum, as well as linearization techniques (digital pre-distortion (DPD), outphasing, envelope tracking, etc.) and efficiency enhancement (load-modulation, supply modulation, etc.).

Speakers:

1. "Phased Array Linearization for mm-Wave 5G and 6G Infrastructure Transmitters", **Raja N. Mir**, *Nokia*
2. "mm-Wave and Sub-THz Power Amplifiers? Enabling Technologies for Beyond-5G and 6G Wireless Networks", **Hua Wang**, *Georgia Tech*
3. "Innovative Integrated Solutions for mm-Wave 5G Front-Ends, Combining 150nm GaN PA with GaAs Receiver", **Eric Leclerc, Mohammed Ayad**, *UMS*
4. "High Performance GaN MMIC Technology for Broadband and mm-Wave Power Amplifiers", **David Brown**, *BAE Systems*
5. "Digital Predistortion for Massive MIMO Phased Array Transmitters", **Anding Zhu**, *University College Dublin*
6. "Control and Linearization of Dual Input Doherty, Chireix and Hybrid PAs", **Yunsik Hahn, Patrick Roblin**, *The Ohio State University*
7. "Challenges in Power Amplifier Design in RFIC-MMIC Technology", **Karun Rawat**, *IIT Roorkee*
8. "Broadband Highly Efficient and Linear 5G mm-Wave PAs in Advanced III-V and Silicon Technologies", **Donald Y.C. Lie**, *Texas Tech University*
9. "Analog-Digital Predistortion Techniques for Multi-Band-Broadband Power Amplifiers", **Meenakshi Rawat**, *IIT Roorkee*

Workshop WSH (half day, 10:00–14:00)
MIMO and Digital Beamforming Systems for 5G and Beyond

Sponsor: **RFIC**

Organizers: **Kamran Entesari**, *Texas A&M University*
Arun Natarajan, *Oregon State University*

Abstract: 5G networks target order-of-magnitude increase in data traffic to support growing demand in mobile networks. Massive multiple-input, multiple-output (MIMO) technology will increase capacity by delivering high data rates to multiple users, support real-time multimedia services and reduce energy consumption by targeting signals to individual users utilizing digital beamforming. Additionally, element-level digital beamforming that supports emerging multi-beam communications and directional sensing will expand the use of mm-wave arrays and make them broadly applicable across Department of Defense (DoD) systems. The focus of this workshop is to present state-of-the-art radio circuits and systems exploiting MIMO and digital beamforming for both civilian 5G NR and defense applications. Talks will focus on development of digital beamformers as well as efficient implementation and packaging of MIMO arrays at RF and mm-wave.

Speakers:

1. "Scalable, Reconfigurable Multi-Layer Hybrid-Digital MIMO Transceiver for TDD-FDD and Full-Duplex Communication", **Jeyanandh Paramesh**, *Carnegie Mellon University*
2. "MIMO Transceivers for 5G and Beyond", **Walid Y. Ali-Ahmad**, *Samsung*
3. "mm-Wave Digital Arrays: Emerging Technologies for Wideband Arrays", **Timothy M. Hancock**, *DARPA*
4. "Architectures for Scalable MIMO Transceivers at RF and mm-Wave", **Harish Krishnaswamy**, *Columbia University*

Workshop WSI (half day, 10:00–14:00)
mm-Wave Phased-Array Transceiver Design: From Basics to Advancements

Sponsor: **RFIC**

Organizers: **Bodhisatwa Sadhu**, *IBM T.J. Watson Research Center*
Kenichi Okada, *Tokyo Institute of Technology*

Abstract: The tutorial-style workshop by top phased-array experts in academia and industry will provide an in-depth learning experience for the attendees and walk them through the different aspects of mm-wave phased-array transceiver design. The workshop will cover the following topics on mm-wave phased arrays: (1) silicon-based mm-wave phased-array basics, (2) phase and gain

control circuits, (3) phased-array antenna and antenna interface design, (4) package, antenna and module co-design and calibration for the end-to-end design, (5) phased-array measurements: on-chip and over-the-air, and (6) current 5G NR phased-array systems, limitations, and an outlook toward 6G.

Speakers:

1. "Radiofrequency and mmWave Phased Arrays", **Hossein Hashemi**, *University of Southern California*
2. "Phased Array Building Blocks, ICs, and Packaging/Module Integration", **Alberto Valdes-Garcia**, *IBM T.J. Watson Research Center*
3. "mmWave Phased Array Testing: The Flow from Initial Debug to High Volume Production", **Mustapha Slamani**, *GLOBALFOUNDRIES*
4. "mmWave Multi-Antenna/MIMO Techniques for 5G NR", **Bo Hagerman**, *Ericsson*

Workshop WSJ (half day, 10:00–14:00)
Recent Advances in Frequency Generation Techniques for sub-6GHz, mm-Wave, and Beyond

Sponsor: **RFIC**

Organizers: **Wanghua Wu**, *Samsung*
Ruonan Han, *MIT*

Abstract: In emerging 5G cellular communication and other mm-wave systems, the generation, distribution, and synchronization of the local oscillator (LO) signals remain a challenge. This workshop covers the latest design techniques of frequency synthesis circuit components and systems to generate LO signals with low phase noise, low spurious tones, fast hopping, and long term stability across a wide operation frequency range. The first talk focuses on LO frequency synthesis and VCO coupling mitigation in the advanced 5G cellular transceiver. The second talk focuses on ultra-wide-tuning-range VCO design for mm-wave and sub-THz frequencies. The third talk discusses the design challenge and techniques for broadband fast Hopping DDFS. And the last talk introduces a new low cost reference clock generation method, molecular clock, for wireless network synchronization and navigation.

Speakers:

1. "Ultra-Wide-Tuning-Range CMOS mm-Wave and Sub-THz VCOs", **Howard C. Luong**, *HKUST*
2. "Digitally-Intensive Subsampling PLLs for FMCW Radar Applications", **Nereo Markulic**, *imec*
3. "Chip-Scale Molecular Clock: Accurate Timestamps from a Molecular Beat", **Cheng Wang**, *MIT*
4. "5G Sub-6GHz LO Frequency Synthesis, VCO Coupling Mitigation and On-Off Disturbance Reduction", **Chih-Wei Yao**, *Samsung*

Workshop WSK (full day, 10:00–16:00)
Satellite Systems: A Top-Down Review of Satellites, Space Communication and Hardware

Sponsor: **RFIC**

Organizers: **Tim LaRocca**, *Northrop Grumman*
Steven E. Turner, *BAE Systems*

Abstract: Want to understand the "Go" in GoGo Wireless In-flight Satellite Internet? Interested in learning about satellite orbits, link budgets, CubeSats and its demands on RF electronics? Need to design on CMOS using a high-reliability PDK or next generation rad-hard process? This vertically oriented workshop provides technical know-how from the satellite to the device by bringing together commercial and defense leaders in space hardware. A review of satellite orbits and the demands on the antenna system as well as a detailed overview of CubeSats and the drive for small-form factor, high reliability electronics is covered. This is followed by a comprehensive review of the market and challenges for SatCom terminals and the need for high reliability electronics. The workshop will then cover RFICs for space in both CMOS and III-V technology including a special overview of advanced very low power CMOS for deep space sensors. Finally, a technical review of radiation types, effects on CMOS, and the techniques to successfully design in space using a radiation hard library or a next generation radiation hard process on advanced bulk CMOS is offered. This is a great place for new and experienced engineers to learn about the adventure of space.

Speakers:

1. "High Level RF Requirements for Commercial Space Systems", **William Caven**, *Maxar*
2. "Designing for the Form-Factor: Key Considerations from Both CubeSat and SmallSat Perspectives", **Adam Gunderson**, *Northrop Grumman*
3. "SatCom Terminal Market Overview and Challenges", **Bill Milroy**, *ThinKom*
4. "A New CubeSat Design with Reconfigurable Multi-Band Radios for Dynamic Spectrum Satellite Communication Networks", **Ian Akyildiz**, *Truva*
5. "RF CMOS for Space Science", **Adrian Tang**, *Jet Propulsion Laboratory*
6. "CMOS RF for Very High Reliability Applications", **Purushothaman Srinivasan, Fernando Guarin**, *GLOBALFOUNDRIES*
7. "Rad Hard by Design: A Necessity for Today's Critical Space Missions", **Jason Ross**, *BAE Systems*
8. "Creating Radiation-Hard CMOS Technology with HARDSIL", **Patrice Parris**, *VORAGO Technologies*

Workshop WSL (half day, 10:00–14:00)
Sub-6GHz Advanced Transmitter Architectures and PA Linearization Techniques

Sponsor: **RFIC**

Organizers: **Jennifer Kitchen**, *Arizona State University*
Antoine Frappé, *IEMN (UMR 8520)*
Raja Pullela, *MaxLinear*

Abstract: 5G communications in the sub-6GHz frequencies offer enhanced data rates, capacity, and flexibility but face challenges such as energy efficiency, linearity, integration, and scalability. To increase battery life, optimization of the efficiency of the power amplifier is of utmost importance. This workshop investigates digitally intensive transmit architectures and pre-distortion techniques that enhance the efficiency of transmitters and power amplifiers used in these next-generation wireless systems. Experts from industry and academia will share their latest research on linearization techniques to build highly efficient linear PAs in various technologies employing topologies such as Doherty, out-phasing, or polar. Circuit topologies and digital signal processing algorithms for pre-distortion of these power amplifiers will also be covered in this workshop.

Speakers:

1. "Wideband Bits-in RF-out CMOS Transmitters", **Leo de Vreede, Morteza S. Alavi**, *Technische Universiteit Delft*
2. "Sub-6GHz SOI-CMOS High-Efficiency Linear PA Architectures: Challenges, Techniques, and Opportunities", **Ayssar Serhan**, *CEA-Leti*
3. "Radio Base Station Transmitters", **Rui Hou**, *Ericsson*
4. "Integrated Digital RF Transmitters with Single-Bit Delta-Sigma-Driven FIR-DACs", **Andreas Kaiser, Antoine Frappé**, *IEMN (UMR 8520)*
5. "Doherty PA Solutions for sub-6GHz mMIMO and Considerations for Improved DPD Linearizability", **Margaret Szymanowski[1], Joe Staudinger[2]**, *[1]Crane Aerospace & Electronics, [2]NXP Semiconductors*
6. "Digital Predistortion: Principles, Techniques, and Trends", **Patricia Desgreys, Germain Pham**, *Télécom Paris*
7. "Digital Intensive Outphasing Transmitters – Design for Wideband Linear Response", **Jussi Ryynänen**, *Aalto University*
8. "Advances in Digitally Intensive Integrated CMOS Transmitters for WiFi and LTE Applications", **Ashoke Ravi, Ofir Degani**, *Intel*

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