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SNUG SILICON VALLEY 2022

AGENDA AT A GLANCE

DAY 1 | MARCH 30, 2022

	2.5D AND 3D MULTI-DIE SYSTEM DESIGN	AI AND MACHINE LEARNING	AUTOMOTIVE	ANALOG/MIXED SIGNAL DESIGN AND SIMULATION	DESIGN AND VERIFICATION IN THE CLOUD	DIGITAL DESIGN IMPLEMENTATION	LOW POWER	PHYSICAL VERIFICATION CHALLENGES AND SUCCESS	SECURITY, DEFENSE & AEROSPACE	SIGNOFF	SILICON TEST AND ANALYTICS	SUCCESSFUL IP INTEGRATION INTO SOCS	VERIFICATION HARDWARE (INCL. EMULATION, PROTOTYPING)	VERIFICATION SOFTWARE SIMULATION & DEBUG	VERIFICATION SOFTWARE STATIC AND FORMAL VERIFICATION
8:00 AM–8:50 AM									**User Presentation:** Hide and Seek: Exploring the Frontiers of Hardware Security Using Synopsys tools.	**User Presentation:** A Pragmatic Approach to High-Accuracy Standard Cell Parasitic Extraction Modeling on Intel 4 technology	**Synopsys Sponsored: Track Keynote:** The Importance of Optimizing Silicon and Systems by Leveraging Test to In-Field				
			User Presentation: Efficient Dual Core LockStep Processor Design with ASIP Designer: An ST STxP5 Case Study						**User Presentation:** Cryogenically Cooled Electric Power Train for Electrified Aircraft Propulsion	**Synopsys Sponsored:** ESP Power Aware Library Formal Verification Sign Off with NVIDIA Standard Cell Library	**Tutorial:** Streaming Fabric and Sequential Compression: Breakthrough Test Time and Test Data Reduction				
9:00 AM–10:00AM	**KEYNOTE:** Catalyze the Impossible **Dr. Aart de Geus, Synopsys,Inc.**														
10:00 AM–11:00 AM	**Tutorial:** Leveraging Die-to-Die IP to Demystify the World of 3DIC Design		**Synopsys Sponsored:** Fault Injection Verification on World's First ASIL D Ready RISC-V Vector Extension Processor—a NSITEXE Case Study	**Tutorial:** Design and Verify State-of-the-Art RF ICs Using the Synopsys Custom Design Platform	**Synopsys Sponsored:** Rapidly Scale and Reduce Time-to-Market for Your Designs Using Synopsys Products in Public Cloud	**Tutorial:** DTCO Methodology for improving Routability in Advanced Process Nodes	**Synopsys Sponsored:** Low Power Technologies in RTL2GDS Flow	**User Presentation:** Once-A-Day Full Chip Physical Verification for Reticle size chips in 7nm using IC Validator and IC Workbench	**User Presentation:** Security: Next Dimension in SysMoore complexity for Overall System Design	**Synopsys Sponsored:** Improving Design Robustness by Addressing Aging Sensitive Paths Using STA Aging Solution	**Tutorial:** A Practical Approach to DFT for Large SoCs and AI Architectures	**Tutorial:** How New HPC Trends Are Influencing High-Speed SerDes IP	**User Presentation:** Unifying Emulation and FPGA Build to Meet Hardware and Software Validation Needs	**User Presentation:** Demystifying Error Injection in UVM Testbench	**Tutorial:** Comprehensive Functional Lint analysis Enabling Lowest Noise Leveraging Formal Technology
	User Presentation: Bump Planning Framework For Concurrent Design Of C4s And Microbumps In Intel 3DIC Foveros based designs		**Synopsys Sponsored:** Valens' MIPI Automotive Camera IP Use Case		**Synopsys Sponsored:** Unleashing Cloud's Potential: Taking Your Chip's Design and Verification to the Cloud	**Synopsys Sponsored:** Simulation Based Standard Cell Routability Analysis		**User Presentation:** Full Chip Physical Signoff for Connectivity and Ultra-high bandwidth Designs	**User Presentation:** ZS4 SoC Digital Twin as a Microelectronic Security Research Testbed	**User Presentation:** Accurate Aging-Aware Robustness with Machine-Learning Speed-up	**User Presentation:** Design for Test and ATPG Strategy for a Large ML SoC		**User Presentation:** "Shift left" using Industry's Fastest Emulator	**User Presentation:** Dynamic MCP (Multi-cycle Path) Verification in VCS	**Tutorial:** Ensuring Zero Chip-killing Bugs for Complex Designs with Scalable RDC Strategies
11:00 AM–11:15 AM	NETWORKING BREAK														
11:15 AM–12:15 PM	**Tutorial:** Synopsys 3DIC Multi-die Convergent Signoff with PrimeTime, StarRC and Tweaker ECO		**Tutorial:** Dependable Product Development Life Cycle for Automotive SoC's in the Context of Overarching Industry Standards like IEEE P02851	**User Presentation:** Automated Register File Construction using Synopsys Custom Compiler	**Synopsys Sponsored:** Azure HBv3 with AMD Milan-X Architectural Advantages for Logic Simulation Using VCS	**User Presentation:** Arm Hierarchical Flow	**User Presentation:** Emulation Based Power Analysis	**User Presentation:** Reduce Physical Signoff Turn-Around-Time using High-Performance Physical Verification with Synopsys IC Validator on Amazon Web Services	**Synopsys Sponsored: Track Keynote:** Manufacturing Next-Generation Microelectronics	**User Presentation:** Cerebras Achieves 4x Improvement in Memory/runtime Over Flat Analysis using HyperGrid Technology	**Synopsys Sponsored:** Accelerating DFT with automated RTL DFT insertion Flow	**Tutorial:** HBM3—A Technical Deep Dive	**Tutorial:** Using ZeBu Cloud4 for RISC-V SoC Emulation	**User Presentation:** Improving SoC Development Flow by Caching EDA Tool Run Results	**Tutorial:** Achieve Best Efficiency for Static Signoff with Multi-mode CDC Analysis
	User Presentation: Achieving Multi-die and Package Co-design Productivity with 3DIC Compiler		**Tutorial:** Is Your Automotive Reliable? Security is Critical Piece for Safe and Reliable Car	**User Presentation:** NVIDIA GPUs Enables Faster IC Simulations & Signoff	**Synopsys Sponsored:** RTL-to-Signoff Digital Design Solution on Cloud	**User Presentation:** P&R Prototype: Dirty Data Handling Related to Incomplete RTL and DFT Constraints using Integrated RTLA and TestMAX Advisor	**User Presentation:** Platform UseCase Peak Power and Average Power Analysis Using PrimePower	**User Presentation:** Advances in Silicon Photonics Design Enablement with Synopsys Tools	**Tutorial:** Automating Secured Silicon—The AISS Methodology	**User Presentation:** IR Aware STA	**User Presentation:** TestMAX Advisor for Powerful and Easy Checking of Pipeline and Other Signal Connections		**Tutorial:** Synopsys Pre-silicon BSA compliance Testing and Performance Verification Solution for Arm SoC	**Tutorial:** Enhance Debug Efficiency up to 10X with Verdi Intelligent Debug Accelerator (IDX)	**Tutorial:** Build High Quality RTL for Power, Placement and Area (PPA) Closure with RTL Architect
12:15 PM–12:30 PM	NETWORKING BREAK														
12:30 PM–1:30 PM	**SPOTLIGHT PANELS** **The Vision of 1000x Productivity in Analog Designs**				**EDA on Cloud: Yesterday's Pipe Dream is Today's Reality**						**Robust PPA for HPC Design Implementation and Signoff**				
1:30 PM–1:45 PM	NETWORKING BREAK														
1:45 PM–2:30 PM	**The New Dynamism: Women in Engineering and the Vast Opportunity Ahead**														
2:30 PM–3:30 PM	**Tutorial:** 3DIC Test and Repair		**Tutorial:** Verification and Validation of Automotive Safety SEooC	**Tutorial:** Top Visually-Assisted Layout Automation Features Maximizing Teams' Productivity	**Synopsys Sponsored:** Reduce Physical Signoff Turn-Around-Time Using High Performance Physical Verification with Synopsys IC Validator on Amazon Web Services	**User Presentation:** Building Source Sync Clocks in System-On-Chip Designs	**User Presentation:** Dynamic IR Drop Analysis	**Tutorial:** Debugging Physical Verification Results: Tips for Smart Debugging	**User Presentation:** Secure Design and Fabrication: A Synopsys-FICS Collaboration	**User Presentation:** IR Drop Fixing using Timing ECO Integrated Solution with IR Signoff Tool	**User Presentation:** A Unified Memory BIST Diagnostics and Failure Analysis Flow	**Tutorial:** PCIe 6.0 New Features, Security Options, Emerging Applications		**Tutorial:** Improve Verification Productivity with VCS Dynamic Test Loading	
			Tutorial: Automated Method for Obtaining Failure Mode Distribution: A DesignWare ARC Processor Case Study		**User Presentation:** Accelerating Chip Design on Cloud—Best Practices for Applying DSO.ai™ on Samsung's SAFE™ Cloud Design Platform (CDP)		**User Presentation:** Prioritizing Clock Gating Fixes in a High Performance Design	**Tutorial:** IC Validator Technology Update: Latest Physical Verification Innovations for Fast Closure	**User Presentation:** The Role of EDA in Designing for Hardware Security	**User Presentation:** Achieving Faster TAT using Tweaker Gigachip Hierarchical ECO	**User Presentation:** Design and Implementation of Functional Protocol-based HSIO Test Solution				
3:30 PM–4:30PM	**ENTERTAINMENT & NETWORKING**														
				User Presentation: In-Design Simulation—Partial Layout Extraction with Signoff Tools for Samsung Foundry Advanced Node					**User Presentation:** Demistifying Secure Design	**User Presentation:** A Case Study for Options to Constraint Asynchronous Timing Paths in the STA tool					
				User Presentation: Measuring Crosstalk Pushout Effect using PrimeSim CCK Application											

DAY 2 | MARCH 31, 2022

	2.5D AND 3D MULTI-DIE YSTEM DESIGN	AI AND MACHINE LEARNING	AUTOMOTIVE	ANALOG/MIXED SIGNAL DESIGN AND SIMULATION	DESIGN AND VERIFICATION IN THE CLOUD	DIGITAL DESIGN IMPLEMENTATION	LOW POWER	PHYSICAL VERIFICATION CHALLENGES AND SUCCESS	SECURITY, DEFENSE & AEROSPACE	SIGNOFF	SILICON TEST AND ANALYTICS	SUCCESSFUL IP INTEGRATION INTO SOCS	VERIFICATION HARDWARE (INCL. EMULATION, PROTOTYPING)	VERIFICATION SOFTWARE SIMULATION & DEBUG	VERIFICATION SOFTWARE STATIC AND FORMAL VERIFICATION
8:00 AM–8:50 AM				**User Presentation:** Clock Network Simulation for Early Skew & Latency Closure						**Synopsys Sponsored:** TSMC and Synopsys Collaboration on SiliconSmart Library Characterization for Advanced Nodes	**User Presentation:** Enabling Automated Wafer Map Flow with SiliconDash				
		Synopsys Sponsored: Exploring World of AI-Driven Physical Design Applications	**Tutorial:** Accelerate Automotive Software Development with a Model-Based Approach: An Infineon AURIX TC4x Case Study							**Synopsys Sponsored:** Synopsys and Samsung 3nm StarRC Collaboration to Deliver High-Accuracy QoR for Gate-All-Around Nodes	**User Presentation:** Driving to Entitlement Yield in Foundry and TI Fabs with Synopsys Yield Explorer				
9:00 AM–9:50 AM	**KEYNOTE:** AI and Its Impact on Humanity **Daniela Rus, MIT**														
9:50 AM–10:00 AM	NETWORKING BREAK														
10:00 AM–11:00 AM		**Synopsys Sponsored:** AI's Next Act—Impact on Chip Design Today and Vision for Future	**Tutorial:** ASIL D-Compliant SoC Design with Synopsys' Safety Specification Format (SSF): Automated End-to-End Traceability, Implementation and Verification	**Tutorial:** Significantly Improved Coverage and Productivity Gain for Analog and Mixed-Signal Designs using Industry's First End-to-End Unified Reliability Workflow	**Synopsys Sponsored:** Massive Parallelization in the Cloud: Synopsys Library Characterization on AWS	**Synopsys Sponsored:** Clock Network Simulation for Early Skew and Latency Closure	**User Presentation:** Library Content Benchmarking and Feature Richness for Better Design PPA	**Tutorial:** Physical Verification for Silicon Photonics Designs		**User Presentation:** IR-Drop Aware	**User Presentation:** Implementing HSIO SCAN Test with TestMAX ALE on V93000 ATE	**Tutorial:** AI Accelerators: Edge AI, Cloud AI and On Premises AI	**Tutorial:** Exploring a Software First Approach to Avoid SoC Re-spin	**User Presentation:** Early Use-cases of VCS ICO (Intelligent Coverage Optimization)	**Tutorial:** Formally Guaranteeing SoC Connectivity Correctness by Analyzing Impact of Low Power Logic Insertion
			User Presentation: In-System Automotive Test Solution for External Memories		**Synopsys Sponsored:** Synopsys Defense in Depth Cloud Security Approach and Case Study	**Synopsys Sponsored:** Physical Design Hand Book for Complex Low Power Architecture using Fusion Compiler		**User Presentation:** ICV LVS Explorer for 2x faster PDV of High Performance Designs		**User Presentation:** Using PrimeShield Vt-Skew Feature for Corner Reduction	**User Presentation:** How to Leverage AI to Outperform the Competition		**Tutorial:** Systems Emulation and Validation with ZeBu Memory Transactors	**User Presentation:** Reactive Sequence Methodologies with Multiple Drivers	**User Presentation:** Applying Formal Analysis in Simulation-based Methodology
11:00 AM–11:15 AM	BREAK														
11:15 AM–12:15 PM		**User Presentation:** Leveraging DSO.ai™ to achieve optimized PPA and TAT	**User Presentation:** Efficient In-System BIST for High-Performance, High-Complexity and Low-Power Automotive Designs	**Tutorial:** In-design Electrical Reporting Process for Samsung Advanced Nodes	**Synopsys Sponsored:** PrimeSim Continuum—10X Faster Simulation with GPU on the Cloud	**Synopsys Sponsored:** FPLab: A Parametrized Approach to Ease Floorplan Execution	**User Presentation:** Timing and Physical Aware RTL Power Exploration with Glitch Source Identification			**User Presentation:** Improving Design PPA with PrimeShield Robustness Optimization	**Tutorial:** Path Margin Analysis Enabling the Next Level of Device Observability		**Tutorial:** Keysight's IxVerify Virtual Testing Solution on ZeBu for Networking and 5G ORAN SoCs	**Tutorial:** Enhance Regression Efficiency and Coverage Closure with Execution Manager	**Tutorial:** De-facto Formal Solution for High-quality RTL Signoff—Sequential Equivalence Checking(SEQ)
		Synopsys Sponsored: AI-Driven Voltage and Frequency Optimization : Maximizing Performance and Power for Mobile CPU	**Tutorial:** What's New in Fault Simulation with VC Z01X	**User Presentation:** GlobalFoundries 45SPLCO Monolithic Silicon-Photonics Technology Design Methodology Using Synopsys OptoCompiler Platform	**Synopsys Sponsored:** VCS Hybrid Cloud Implementation Using Pure Storage on Microsoft Azure	**Synopsys Sponsored:** Efficient Planning and Automation of Top Metal Routing and MIMCAP Generation				**Synopsys Sponsored:** Reducing ECO TAT on Very Large Designs with Tweaker Gigachip Hierarchical Flow	**Tutorial:** Silicon Lifecycle Management using SMS for Emerging Memories		**Tutorial:** Virtualizing Multiple interfaces of 5G base station SoC on ZeBu Cloud4	**User Presentation:** Demystifying the UVM Phasing Mechanism	
12:15 PM–12:30 PM	NETWORKING BREAK														
	SPOTLIGHT PANELS														
12:30 PM–1:30 PM	**SoC Leaders Verify with Synopsys**							**3DIC Design: Crossing over from buzz to adoption**							
1:30 PM–1:45 PM	NETWORKING BREAK														
1:45 PM–2:30 PM	**A Conversation with Sassine Ghazi, President & Chief Operating Officer**														
2:30 PM–3:30 PM		**Synopsys Sponsored:** Maximize PPA Benefits using DSO.ai™—Case Studies from Sony Designs		**User Presentation:** Dynamic Analog Configuration Updates in Mixed Signal Simulation		**User Presentation:** Simple & Efficient Binary-to-Gray & Gray-to-Binary Implementations Using SystemVerilog	**Synopsys Sponsored:** Energy Efficient Design			**User Presentation:** Leveraging QuickCap NX Accuracy and StarRC Parasitics Analysis for High Quality IP Library Development	**Synopsys Sponsored:** Silicon Lifecycle Management and What it Means for the Future of Semiconductor Test and SoC Development			**Tutorial:** Simplify UPF Generation and Optimization with Verdi UPF Architect	**Tutorial:** Synopsys Euclide: New Features and Tips for Optimized Workflows
		Synopsys Sponsored: Accelerate Coverage Closure and Expose Testbench Bugs using VCS ML-Driven Intelligent Coverage Optimization Technology				**Tutorial:** PPA(V) Tutorial				**User Presentation:** NanoTime Memory for Register File Designs					
3:30 PM–4:30 PM	**ENTERTAINMENT & NETWORKING**														
				Tutorial: Improvement in PrimeSim GPU Simulation using Samsung Foundry Advanced Node						**User Presentation:** SDC Constraint Pitfalls for the Asynchronous Timing Paths during Asynchronous FIFO design					
				User Presentation: Robust Detection of Leakage Currents for Large SoC Designs											